GATEFLIX

ELECTRONIC DEVICES & CIRCUITS

For

ELECTRONICS & COMMUNICATION ENGINEERING

ELECTRONIC DEVICES & CIRCUITS

SYLLABUS

Energy bands in silicon, intrinsic and extrinsic silicon. Carrier transport in silicon: diffusion current, drift current, mobility, and resistivity. Generation and recombination of carriers.p-n junction diode, Zener diode, tunnel diode, BJT, JFET, MOS capacitor, MOSFET, LED, P-I-N and avalanche photo diode, Basics of LASERs.
Device technology: integrated circuits fabrication process, oxidation, diffusion, ion implantation, photolithography, n-tub, p-tub and twin-tub CMOS process.

ANALYSIS OF GATE PAPERS

Exam Year	1 Mark Ques.	2 Mark Ques.	Total
2003	5	5	15
2004	3	7	17
2005	3	3	9
2006	4	4	12
2007	2	6	14
2008	4	4	12
2009	2	3	8
2010	2	4	10
2011	3	3	9
2012	1	3	7
2013	3	-	3
2014 Set-1	2	5	12
2014 Set-2	3	3	9
2014 Set-3	3	4	11
2014 Set-4	3	4	11
2015 Set-1	2	2	6
2015 Set-2	2	3	8
2015 Set-3	2	2	6
2016 Set-1	3	4	11
2016 Set-2	3	4	11
2016 Set-3	3	3	9
2017 Set-1	3	4	11
2017 Set-2	3	4	11
2018	4	4	12

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1 SEMICONDUCTORS

1.1 STRUCTURE OF AN ATOM

Matter has mass and takes up space. Atoms are basic building blocks of matter, and cannot be chemically subdivided by ordinary means. Atoms are composed of three types of particles: **proton**, **neutron**, and **electron**. Proton and neutron are responsible for most of the atomic mass. The mass of an electron is very small $m_n = 9.108X10^{-31}\,kg$

Both the protons and neutrons reside in the nucleus. Protons have a positive (+) charge, neutrons have no charge i.e. they are neutral. Electrons reside in orbitals around the nucleus. They have a negative charge (-). The electrons of an atom are bound to the nucleus by the electromagnetic force. Likewise, a group of atoms can remain bound to each other by chemical bonds based on the same force, forming a molecule.

An atom containing an equal number of protons and electrons is electrically neutral; otherwise it is positively or negatively charged and is known as an **ion**. It is the number of protons that determines the atomic number.

e.g. no. of protons in the nucleus of silicon is 14 hence atomic no. of Si=14.

All atoms would like to attain electron configurations like noble gases. That is, have completely filled outer shells. Atoms can form stable electron configurations like noble gases by:

1. Losing electrons
2. Sharing electrons
3. Gaining electrons.

For a stable configuration each atom must fill its outer energy level. In the case of noble gases that means eight electrons in the last shell (with the exception of He which has two electrons). Atoms that have 1, 2 or 3 electrons in their outer levels will tend to lose them in interactions with atoms that have 5, 6 or 7 electrons in their outer levels. Atoms that have 5, 6 or 7 electrons in their outer levels will tend to gain electrons from atoms with 1, 2 or 3 electrons in their outer levels. Atoms that have 4 electrons in the outer most energy level will tend to neither totally lose nor totally gain electrons during interactions.

1.2 ENERGY BAND THEORY

In solid-state physics, the electronic band structure (or simply band structure) of a solid describes those ranges of energy that an electron within the solid may have (called allowed or permitted bands), and ranges of energy that it may not have (called forbidden bands).

Out of all the energy bands, three bands are most important to understand the behavior of solids. These bands are,

1) Valence band
2) Conduction band
3) Forbidden band or gap

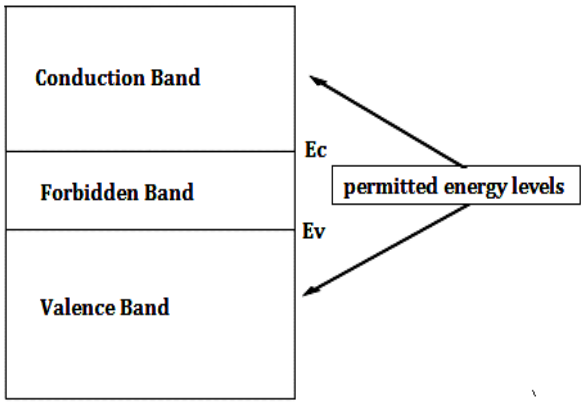


Fig. Energy Band Diagram

The energy band formed due to merging energy levels associated with the valence electrons i.e. electrons in the last shell is called **valence band.** In normal condition,

valence electrons form the covalent bands and are not free. But when certain energy is imparted to them, they become free.

The energy band formed due to merging of energy levels associated with the free electrons is called **conduction band.** Under normal condition, the conduction band is empty and once energy is imparted, the valence electrons jump from valence band to conduction band and become free.

While jumping from valence band to conduction band, the electrons have to cross an energy gap. This energy gap which is present separating the conduction band and the valence band is called **forbidden band** or **forbidden gap.** The energy imparted to the electrons must be greater than the energy associated with the forbidden gap, to extract the electrons from valence band and transfer them to conduction band. The energy associated to forbidden band is denoted as E_G.

The graphical representation of the energy bands in a solid is called **energy band diagram**

Note:-The electrons cannot exist in the forbidden gap.

1.2.1 UNIT OF ENERGY eV

The unit joule is very large for the energies associated with electrons. Hence such energies are measured in electron volts denoted as eV. 1 eV is defined as the kinetic energy gained by an electron when it falls through a potential of one volt.

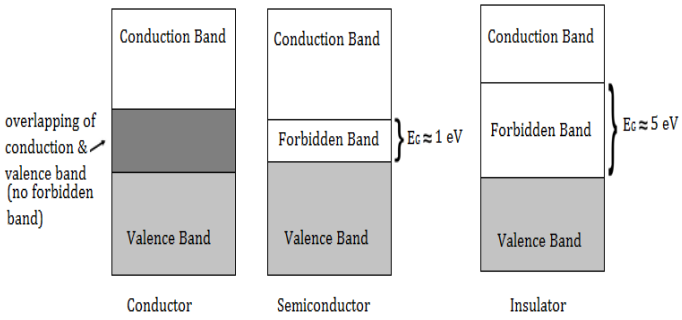
$1\text{eV} = 1.6\times10^{-19}\text{J}$

1.3 CLASSIFICATION OF MATERIALS

Based on the properties shown at different surrounding conditions, materials are classified as

1.3.1 CONDUCTORS

In the metals there is no forbidden gap between valence band and conduction band i.e. $E_G = 0$ eV. The conduction band & valence band are overlapped in conductors**.** Hence even at room temperature, a large number of electrons are available for conduction. So without any additional energy, such metals contain a large number of free electrons and hence called good conductors.



1.3.2 SEMICONDUCTORS

Semiconductors are those materials whose electrical conductivity is between conductors and insulators. The forbidden gap in semiconductors is about 1 eV. In semiconductors the energy provided by heat at room temperature is sufficient to lift electrons from valence band to conduction band. But at T=0 °.k. (absolute zero or -273^{o}C), all the electrons find themselves in valence band hence S.C. behaves as perfect insulators at $T = 0^{o}$K. The forbidden energy band gap in semiconductors depends on temperature & it is given by

$$E_{G\text{ at }T^{o}K} = E_{0^{o}K} - \beta_o T\text{ eV}$$

where,

$\beta_o = 3.6\times10^{-4}\text{eV}/^{o}\text{K}$	for silicon
$\beta_o = 2.2\times10^{-4}\text{eV}/^{o}\text{K}$	for germanium
$E_{0^{o}K} = 1.21\text{eV}$	for silicon
$E_{0^{o}K} = 0.785\text{eV}$	for germanium

Using above equations the forbidden band gap for silicon and germanium at $T = 300^{o}$K i.e. at room temperature are **1.1 eV**&**0.72 eV** respectively.

Example:
E_G for Ge at 0°K = 0.785eV. Calculate E_G at T = 350°K.
Solution:
Given, $E_{GO} = 0.785eV$

$$E_G at T = 350°K = E_{GO} - 2.2\times10^{-4}\times350$$
$$= 0.785 - 2.2\times10^{-4}\times350 = 0.708eV$$

1.3.3 INSULATORS

An insulator has an energy band diagram as shown in the Fig. In case of such insulating material; there exists a large forbidden gap in between the conduction band and the valence band. Practically it is impossible for an electron to jump from the valence band to the conduction band. Hence such materials cannot conduct and called insulators. The forbidden gap is very wide, approximately of about 5 eV.

1.4 FERMI DIRAC FUNCTION

The equations for f(E) is called the Fermi–Dirac probability function, and specifies the fraction of all states at energy E (electron volts) occupied under conditions of thermal equilibrium

$$f(E) = \frac{1}{1+\exp[(E-E_F)/kT]}$$

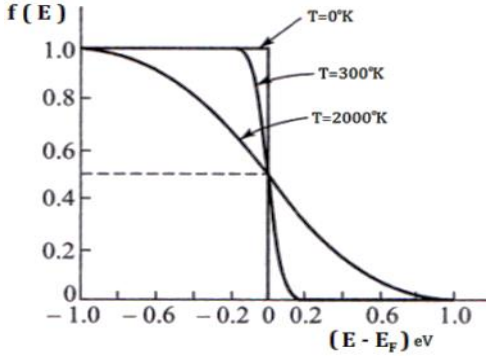
Where,
k = Boltzmann constant, eV/°K
T = Temperature in °K
E_F =Fermi level or characteristic energy in eV

Def: The Fermi level represents the energy state with 50 percent probability of being filled (i.e. 50% probability of finding an electron at this energy level) if no forbidden band exists.

Case-1

If $E = E_F$ then $f(E) = \frac{1}{2}$ for any value of temperature

Case-2:-
When T = 0°K& if $E > E_F$, the exponential term becomes infinite and$f(E) = 0$.
It means at all energy levels above E_F the probability of finding an electron is 0 at$T = 0°K$.
Case-3
When T = 0°K& if $E > E_F$, the exponential term becomes zero and$f(E) = 1$.
It means at all energy levels below E_F the probability of finding an electron is 1 at T = 0°K
A plot of f(E) versus $E - E_F$ is shown in fig

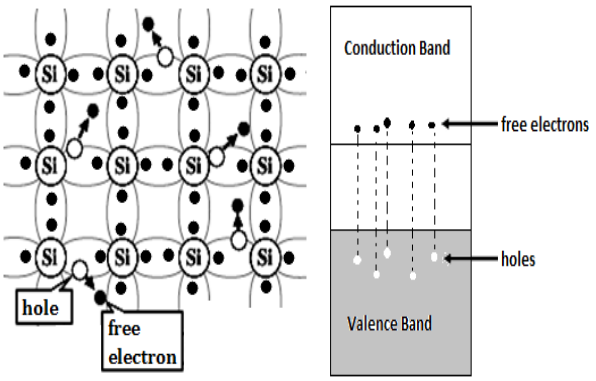


1.5 CLASSIFICATION OF SEMICONDUCTORS

Based on the composition, semiconductors are classified into two types

1.5.1 INTRINSIC SEMICONDUCTOR

In silicon each atom contains 4 valency electrons hence stability is aquired by each atom in the material through sharing of valency electrons. The bonds formed through sharing of electrons in semiconductor are called **covalent bonds**. An intrinsic semiconductor also called an undoped semiconductor or I–type semiconductor is a pure semiconductor without any significant dopant species present. The bond structure of silicon is shown in the fig.



At a very low temperature 0°K no free electrons are available for conduction hence intrinsic semiconductor behaves as perfect insulator. With the increase in temperature, the covalent bonds are broken and electron hole pairs are generated. Such a generation of electron hole pairs due to thermal energy is called **thermal generation.** With the generation electron hole pairs an intrinsic semiconductor starts conducting.

Note:-In intrinsic semiconductor electron concentration is equal to hole concentration i.e.

$$n = p = n_i$$

n_i is called intrinsic carrier concentration & it is given by

$$n_i^2 = A_0 T^3 e^{-E_{G0/kT}}$$

At room temperature,

$n_i = 2.5 \times 10^{13}$ Atoms/cm3 for Germanium

$n_i = 1.5 \times 10^{10}$ Atoms/cm3 for Silicon

Where,

A_0 is material constant

E_{G0} is E_G at $T = 0^oK$

k is Boltzmann's constant

$k = 8.6 \times 10^{-5}$ eV/°K

1.5.11 ELECTRON & HOLE CONCENTRATION

The concentration of electrons in the conduction band can be expressed as

$$n = N_C \exp\left[-(E_C - E_F)/kT\right]$$

Where,

$N_C = 2\left(\frac{2\pi m_n \bar{k} T}{h^2}\right)^{\frac{3}{2}}$ which is called the effective density of states function in the conduction band. m_n is called effective mass of electron. $\bar{k}$ is called Boltzmann's constant

$\bar{k} = 1.381 \times 10^{-23}$ joules /° K

The concentration of hole in valence band can be expressed as

$$p = N_V \exp\left[-(E_F - E_V)/kT\right]$$

Where, $N_V = 2\left(\frac{2\pi m_p \bar{k} T}{h^2}\right)^{\frac{3}{2}}$ which is called the effective density of states function in the valence band. m_p is called effective mass of hole.

1.5.12 FERMI LEVEL

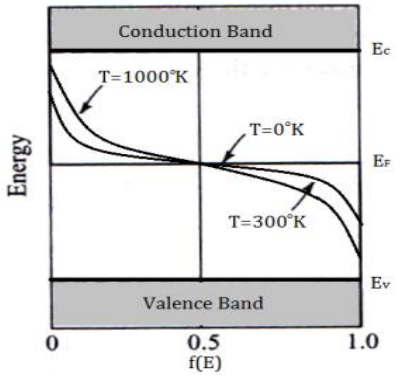
The Fermi level for an intrinsic semiconductor is given by

$$E_F = \frac{E_C + E_V}{2} - \frac{kT}{2} \ln \frac{N_C}{N_V} \quad \ldots(1)$$

If the effective masses of a hole and a free electron are the same i.e. $m_p = m_n$ then $N_C = N_V$,

$$E_F = \frac{E_C + E_V}{2}$$

Putting $T = 0°K$ in above equation we may observe that equation (1) is also valid even for $N_C \neq N_V$. Hence the Fermi level lies in the center of the forbidden energy band.



Example

For a particular semiconductor material, $N_C = 1.5 \times 10^{18} cm^{-3}$, $N_V = 1.3 \times 10^{19} cm^{-3}$ and $E_G = 1.43$ eV at $T = 300°K$

Determine the position of the intrinsic Fermi level with respect to the center of the band gap.

Solution

$$E_F = \frac{E_C + E_V}{2} - \frac{kT}{2}\ln\frac{N_C}{N_V}$$

$$E_{midgap} = \frac{E_C + E_V}{2}$$

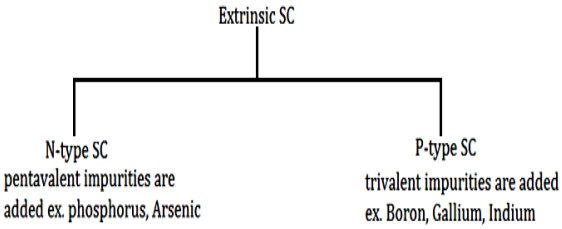
$$E_F - E_{midgap} = \frac{kT}{2}\ln\frac{N_C}{N_V}$$

$$E_F - E_{midgap} = -\frac{0.0259}{2}\ln\left(\frac{1.5\times10^{18}}{1.3\times10^{19}}\right)$$

$$= 0.028\text{eV}$$

Thus the Fermi level is located at 0.028 eV above the center of the band gap.

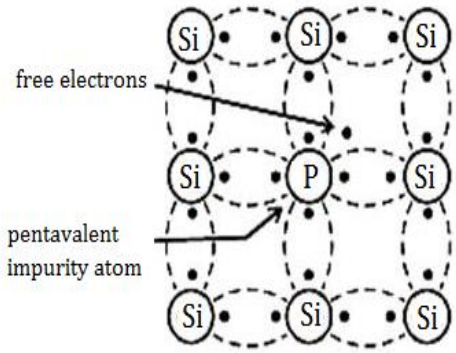
1.5.2 EXTRINSIC SEMICONDUCTOR



1.5.2.1 N-TYPE SEMICONDUCTOR

When a small amount of penta-valent impurity is added to a pure semiconductor, it is called **N-type semiconductor.** The impurity atoms will displace some of the silicon atoms in the crystal lattice. Four of the five valence electrons will occupy covalent bonds, and the fifth will be nominally unbound and will be available as a carrier of current. The energy required to detach this fifth electron from the atom is of the order of only 0.01 eV for Ge or 0.05 eV for Si.

Suitable penta-valent impurities are antimony, phosphorous, and arsenic. Such impurities donate excess (negative) electron carriers, and are therefore referred to as **donor or n-type impurities**.



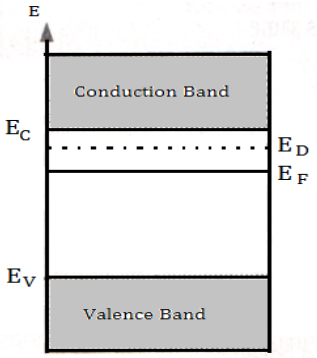
When donor impurities are added to a semiconductor, allowable energy levels are introduced just below the conduction band, as shown in fig. These new allowable levels are essentially a discrete level because the added impurity atoms are far apart in the crystal structure, and hence their interaction is small. In germanium, the distance of the new discrete allowable energy level is only 0.01 eV (0.05 eV in silicon) below the conduction band, and therefore at room temperature almost all of the "fifth" electrons of the donor material are raised into the conduction band.

If intrinsic semiconductor material is "doped" with n-type impurities, not only does the number of electrons increase, but the number of holes decrease below that which would be available in the intrinsic semiconductor. The reason for the decrease in the number of holes is that the larger number of electrons present increases the rate of recombination of electrons with holes.

Note:

1) Donor impurity concentration in an N-type semiconductor is given by
   N_D = Atomic density in semiconductor × Impurity ratio
   Where,
   Atomic density = 4.422 X 10^{22} atmos/ cm^3
   For Germanium
   Atomic density = 5 X 10^{22} atmos/ cm^3
   For Silicon
2) The electrons in N-type SC are called majority charge carriers & holes are called as minority charge carriers.

1.5.2.11 FERMI LEVEL



The Fermi level for N-type semiconductor lies near the conduction band. The position of Fermi level is given by the equation

$$E_F = E_C - kT \ln \frac{N_C}{N_D} eV$$

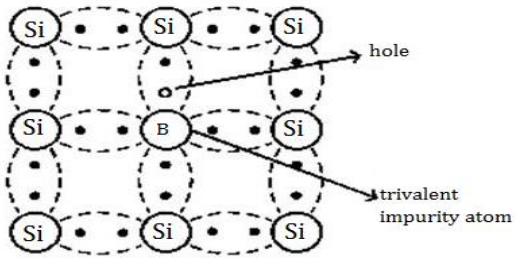
With increase in doping the Fermi level shifts towards conduction band i.e. shift upward with respect to the Fermi level of intrinsic semiconductor. This upward shift is given by

$$E_F - E_{Fi} = kT \ln \frac{N_D}{n_i} eV$$

With increase in temperature the Fermi level of N-type semiconductor shifts towards Fermi level of intrinsic semiconductor & at a very high temperature it coincides with E_{Fi} i.e. at this temperature N-type semiconductor behaves as an intrinsic semiconductor.

1.5.2.2 P-TYPE SEMICONDUCTOR

When a small amount of trivalent impurity is added to a pure semiconductor, it is called **P-type semiconductor.** The trivalent impurity has three valence electrons. The examples of such elements are gallium, boron or indium, such an impurity is called **acceptor impurity.**



Consider the formation of p-type material by adding boron into silicon (Si). The Boron atom has three valence electrons. So Boron atom fits in the silicon crystal in such a way that it's three valence electros from covalent bonds with the three adjacent silicon atoms. Being short of one electron, the fourth covalent bond in the valence shell is incomplete. The resulting vacancy is called a hole. Such p-type material formation is represented in the Fig .This means that each gallium atom added into silicon atom gives one hole. The number of such holes can be controlled by the amount of impurity added to the silicon. As the holes are treated as positively charged, the material is known as p-type material.

At room temperature, the thermal energy is sufficient to extract an electron from the neighboring atom which fills the vacancy in the incomplete bond around impurity atom. But this creates a vacancy in the adjacent bond from where the electron had jumped, which is nothing but a hole. This indicates that a hole created due to added impurity is ready to accept an electron and hence is called acceptor impurity.

Note:

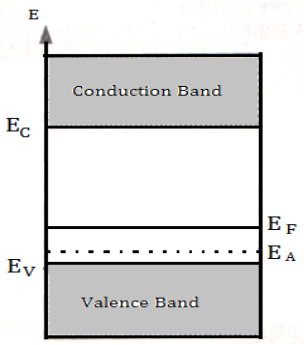
1) Acceptor impurity concentration in an P-type semiconductor is given by
   N_A =Atomic density in semiconductor × Impurity ratio
   Where,
   Atomic density = 4.422×10^{22} atmos/cm^3 for Germanium
   Atomic density = 5×10^{22} atmos/cm^3 for Silicon
2) The holes in P-type SC are called majority charge carriers & electrons are called as minority charge carriers.

1.5.2.21 FERMI LEVEL

The Fermi level for P-type semiconductor lies near the valence band. The position of

Fermi level is given by the equation

$$E_F = E_V + kT \ln \frac{N_V}{N_A} eV$$



With increase in doping the Fermi level shifts towards valence band i.e. shift downward with respect to the Fermi level of intrinsic semiconductor. This downward shift is given by

$$E_{Fi} - E_F = kT \ln \frac{N_A}{n_i} eV$$

With increase in temperature the Fermi level of P-type semiconductor shifts towards Fermi level of intrinsic semiconductor & at a very high temperature it coincides with E_{Fi} i.e. at this temperature p-type semiconductor behaves as an intrinsic semiconductor.

1.6 MOBILITY OF CHARGE CARRIERS

Consider a material is subjected to an external electric field E Volts/m. As a result of electrostatic force, the charge carriers start moving in a definite direction. The velocity of these charge carriers is called drift velocity. This velocity of charge carriers is directly proportional to the applied electric field

$$v_d \propto E \Rightarrow v_d = \mu E$$

Where μ is constant of proportionality and is called mobility of the electrons. This is applicable to the free electrons as well as the holes.

So in general,

Mobility of a charged particle

$$\mu = \frac{v_d}{E} \frac{m^2}{V - sec}$$

At room temperature the mobility of electrons and holes are

mobility	germanium	silicon
μ_n	$3800 \frac{cm^2}{V-sec}$	$1300 \frac{cm^2}{V-sec}$
μ_p	$1800 \frac{cm^2}{V-sec}$	$500 \frac{cm^2}{V-sec}$

1.6.1 EFFECT OF TEMPERATURE

At any temperature above absolute zero, the vibrating atoms create pressure (acoustic) waves in the crystal, which are termed phonons. Like electrons, phonons can be considered to be particles. A phonon can interact (collide) with an electron (or hole) and scatter it. At higher temperature, there are more phonons, therefore increased phonon scattering which tends to reduce mobility i.e. with increase in temperature mobility of charge carriers decreases.

1.6.2 EFFECT OF DOPING

Semiconductors are doped with donors and/or acceptors, which are typically ionized, and are thus charged. The Columbic forces will deflect an electron or hole approaching the ionized impurity. This is known as ionized impurity scattering. The amount of deflection depends on the speed of the carrier and its proximity to the ion. The more heavily a material is doped, the higher the probability that a carrier will collide with an ion in a given time, and the smaller the mean free time between collisions, and the smaller the mobility i.e. with increase in doping the mobility of charge carries decreases.

Example

A bar of silicon 1 cm long is subjected to a potential difference of 20 v. If the velocity of electrons in bar is 250m/s. Determine the mobility of electrons.

Solution

Given,

$$\ell = 1cm = 1 \times 10^{-2} m$$

$$V = 20 volts$$

$V = 250 m/sec$

We know,

$$\text{Mobility } \mu = \frac{v}{E}$$

$$\text{electric field}(E) = \frac{V}{\ell} = \frac{20}{1\times10^{-2}}$$

$$= 2000\, V/m$$

$$\therefore \mu = \frac{250}{2000} = 0.125\, m^2/v-sec$$

$$= 1250\, cm^2/v-sec$$

1.7 LAW OF ELECTRICAL NEUTRALITY

Statement: It states that a semiconductor is always electrically neutral i.e. total positive charge in semiconductor is equal to total negative charge.

Let N_D be the concentration of donor atoms which donate electrons and become positively charged ions. Hence we can say that N_D is concentration of positively charged immobile ions contributed by donor atoms.

Total positive charge density $= N_D + p$

where p is concentration of holes i.e. positive charges

Similarly, N_A is the concentration of acceptor atoms which accept electrons and becomes negatively charged ions. Hence we can say that N_A is the concentration of negative ions contributed by the acceptor atoms.

Total negative charge density $= N_A + n$

where n is concentration of electrons i.e. negative charges.

Since the semiconductor is electrically neutral, the magnitude of positive charge density must equal to that of negative charge density.

$\therefore \quad N_D + p = N_A + n$

Case-1

In n-type material, $N_A = 0$ and the number of holes is much smaller than number of electrons i.e. p<<n. Hence neglecting p, the equation reduce to,

$$N_D \cong n$$

Case-2

In p-type material, $N_D = 0$ and the number of electrons is much less than number of holes i.e. n<<p. Hence neglecting n, the equation reduces to,

$$N_A \cong p$$

1.8 MASS ACTION LAW

Statement: If n is the concentration of free electrons and p is the concentration of holes then the law of mass action states that the product of concentrations of electrons and holes is always constant & it is square of intrinsic carrier concentration. Mathematically,

$$np = n_i^2$$

Where n_i is intrinsic concentration.

The law can be applied to both intrinsic and extrinsic semiconductors.

Case-1

In N-type SC

$$n_n \times p_n = n_i^2$$

$$\therefore p_n = \frac{n_i^2}{n_n} = \frac{n_i^2}{N_D}$$

Using above equation we can calculate the value of p_n i.e. concentration of holes in N-type material (minority carrier concentration in N-type)

Case-2

In P-type SC

$$n_p \times p_p = n_i^2$$

$$\therefore n_p = \frac{n_i^2}{P_p} = \frac{n_i^2}{N_A}$$

Using above equation we can calculate the value of n_p i.e. concentration of electrons in P-type material (minority carrier concentration in P-type)

Note: Mass action law can be used to calculate concentration of minority carriers in extrinsic semiconductors.

1.9 CONDUCTIVITY

Conductivity of a material is defined as the product of carrier concentration, charge of carriers & their motilities.

conductivity(σ) = charge carrier concentration × charge of carriers × mobilty

$\sigma = nq\mu_n + pq\mu_p \text{siemens/m}$

1.9.1 CONDUCTIVITY OF INTRINSIC SEMICONDUCTOR

We know that,

$\sigma = (n\mu_n + p\mu_p)q$

But in intrinsic semiconductor, the electron hole pairs are generated and at any instant number of free electrons is same as number of holes.

i.e. $n = p = n_i$

Substituting in above equation,

$\sigma_i = n_i q(\mu_n + \mu_p) \ldots\ldots (1.17)$

Where σ_i is conductivity of intrinsic semiconductor.

Note: With increase in temperature, mobility of electrons & holes decreases but at the same time there is large increase in electron &hole concentration hence the conductivity of intrinsic semiconductor increases with temperature i.e. conductivity of intrinsic semiconductor has positive coefficient of temperature.

1.9.2 CONDUCTIVITY OF N-TYPE SEMICONDUCTOR

In n-type of material, the free electrons are majority carriers and the holes are minority carriers. When donor impurity is added to the intrinsic semiconductor, donor atom donates electron to the conduction band and becomes positively charged ion.

Let

N_D = Concentration of donor atoms

n = Concentration of free electrons in n-type material

P = Concentration of holes in n-type material.

We know, $\sigma = (n\mu_n + p\mu_p)q$

But the concentration of holes in a n-type semiconductor is very less as compared to the concentration of free electrons i.e. $P_n \ll n_n$. Hence neglecting P_n we can write

$\sigma_n = n\mu_n q$

Now practically all the donor atoms added release their fifth electron as a free electron at room temperature. Hence concentration of donor atoms (N_D) added is approximately equal to the concentration of free electrons in n-type material (n_n) i.e.

$n_n \cong N_D$

Hence conductivity of n-type material is,

$\sigma_n = N_D \mu_n q$

Note: With increase in temperature the mobility of charge carriers decreases by large value in a doped semiconductor, hence conductivity of N-type semiconductor decrease with temperature i.e. conductivity in N-type semiconductor has negative coefficient of temperature.

1.9.3 CONDUCTIVITY OF P-TYPE SEMICONDUCTOR

In p-type of material, the holes are majority carriers and the free electrons are minority carriers. When acceptor impurity is added to the intrinsic semiconductor, acceptor atom accepts an electron to become negatively charged ion.

Let

N_A = Concentration of acceptor atoms

n_p = Concentration of free electrons in p-type material

P_P = Concentration of holes in p- type material

We know, $\sigma = (n\mu_n + p\mu_p)q$

But the concentration of electrons in p-type materials is very much less as compared to the concentration of holes i.e. $n_p \ll P_P$.

Hence neglecting n_p we can write,

$\sigma_p = P_P \mu_p q$

Now practically all the acceptor atoms added accept the electron and produce hole. Hence concentration of acceptor atoms (N_A) is approximately equal to the concentration of holes in P-type material (P_P) i.e. $P_p \cong N_A$

Hence conductivity of p-type material is,

$$\sigma_p = N_A \mu_p q$$

Note: With increase in temperature the mobility of charge carriers decreases by large value in a doped semiconductor, hence conductivity of P-type semiconductor decrease with temperature i.e. conductivity in P-type semiconductor has negative coefficient of temperature.

Example

Find conductivity of N-type Semiconductor with Donor impurity concentration 10^{18} atoms/ cm^3 & mobility of electrons $3800 cm^2/v-sec$

Solution:

Given,

$$N_D = 10^{18} atoms/cm^3$$

$$\mu_n = 3800 cm^2/v-sec$$

$$\sigma = N_D q \mu_n$$

$$= 10^{18} \times 1.6 \times 10^{-19} \times 3800$$

$$= 608 s/m$$

1.10 RESISTIVITY

Resistivity is the reciprocal of conductivity i.e.

$$\rho = \frac{1}{\sigma} \Omega - m$$

1.10.1 RESISTIVITY OF INTRINSIC SEMICONDUCTOR

For intrinsic semiconductor conductivity is given by

$$\sigma_i = n_i q(\mu_n + \mu_p) 3$$

$$\therefore \rho = \frac{1}{n_i q(\mu_n + \mu_p)}$$

Note: Resistivity of intrinsic semiconductor has negative coefficient of temperature.

1.10.2 RESISTIVITY OF N-TYPE SEMICONDUCTOR

For N-type semiconductor conductivity is given by

$$\sigma_n = N_D \mu_n q$$

$$\therefore \rho = \frac{1}{N_D q \mu_n}$$

Note: Resistivity of N-type semiconductor has positive coefficient of temperature.

1.10.3 RESISTIVITY OF P-TYPE SEMICONDUCTOR

For N-type semiconductor conductivity is given by

$$\sigma_p = N_A \mu_p q$$

$$\therefore \rho = \frac{1}{N_A \mu_p q}$$

Note: Resistivity of P-type semiconductor has positive coefficient of temperature.

1.11 RESISTANCE

Resistance of a material is defined as

$$R = \rho l / A \Omega$$

Where,

ρ is the resistivity of material

l is the length of material

A is cross-sectional area of the material

Example

A bar of intrinsic silicon has a cross sectional area of $2.5 \times 10^{-4} m^2$. The electron density is $1.4 \times 10^{16}/m^3$. How long the bar be if I=1.2mA when 9 volts is applied across it. The mobility of electros & holes are $0.14 m^2/vsec$ & $0.05 m^2/vsec$ resp.

Solution:

We know that,

$$R = V/I = 9/1.2 \times 10^{-3} = 7.5 k\Omega$$

Now,

$$R = \rho \ell / A$$

$$\rho = \frac{1}{n_i \times q\left(\mu_n + \mu_p\right)}$$
$$= \frac{1}{1.4\times10^{16}\times1.6\times10^{-19}\left(0.14+0.05\right)}$$
$$= 2349.62\Omega - m$$
$$\ell = \frac{R\times A}{\rho} = \frac{7500\times2.5\times10^{-4}}{2349.62}$$
$$= 0.79mm$$

1.12 CONDUCTANCE

Conductance of the material is the reciprocal of its resistance i.e.

$G = 1/R$ ℧

$\Rightarrow \quad G = A/\rho l$

$\Rightarrow \quad G = \sigma A/l$

Where,

σ is the conductivity of material

l is the length of material

A is cross sectional area of the material

1.13 CURRENT DENSITY

The current density J is defined as the current per unit area of the conducting medium.

$$J = \frac{I}{A} Amp/m^2$$

1.13.1 DRIFT CURRENT

When conductor is subjected to an external voltage, free electrons move from negative to positive terminal & holes moved from positive to negative terminal with a steady velocity constituting a current. Such a current is called drift current which is due to drifting under the effect of external voltage.

1.13.2 DIFFUSION CURRENT

Consider a semiconductor, along its length, in the direction of x as shown in fig; there decrease in the concentration of electrons. As we move from x_1 to x_2 there is decrease in electron concentration i.e. there exist a concentration gradient $\frac{dn}{dx}$. Due to such concentration gradient, electrons move from the higher concentration area to the lower concentration area to adjust the concentration. Such a movement of electrons, due to the concentration gradient in a semiconductor is called diffusion. Due to the movement of electrons, current is constituted in a bar which is called diffusion current. This is the characteristic of semiconductors and cannot be observed in conductors.

1.13.21 DIFFUSION LENGTH

Diffusion length is the average length a carrier moves between generation and recombination. Mathematically it is given by $L = \sqrt{D\tau}$

Where,

D is diffusion constant

τ is minority carrier lifetime

Note:

1) Minority carrier lifetime is the average time between generation & recombination of minority charge carriers
2) Semiconductor materials that are heavily doped have greater recombination rates and consequently, have shorter diffusion lengths.
3) Higher diffusion lengths are indicative of materials with longer lifetimes, and are therefore an important quality to consider with semiconductor materials.

1.13.3 DRIFT CURRENT DENSITY

The drift current density is expressed as,

$J = \sigma E$

Where,

σ is conductivity and is measured in $\left(\Omega - m\right)^{-1}$

E is applied electric field expressed in V/m

1) Electron drift current density is given by $J_n = nq\mu_n E$

2) Hole drift current density is given by
$J_p = pq\mu_p E$

1.13.4 DIFFUSION CURRENT DENSITY

The diffusion current density is proportional to the concentration gradient
i.e. $J_p \propto \frac{dp}{dx}$ & $J_n \propto \frac{dn}{dx}$
Where,
J_p is diffusion current density due to holes
J_n is diffusion current density due to electrons

1) The hole diffusion current density is given by,
$J_p = -qD_p \frac{dp}{dx}$
where, D_p is diffusion constant for holes expressed in m^2/sec
2) The electron diffusion current density is given by,
$J_n = +qD_n \frac{dn}{dx}$
where, D_n is diffusion constant for electrons expressed in m^2/sec

1.13.5 TOTAL CURRENT DENSITY

The drift current is due to the applied voltage while the diffusion current is due to the concentration gradient & in semiconductor it is very much possible that both the types of currents may exist simultaneously.
Total current density due to the electrons is
$J_n = nq\mu_n E + qDn\frac{dn}{dx}$
And total current density due to the hoes is,
$J_p = pq\mu_p E - qDp\frac{dp}{dx}$

Example

Calculate the diffusion current in a piece of germanium having concentration gradient of 1.5×10^{22} electrons$/m^4$ & $D_n = 0.0012 m^2/s$

Solution

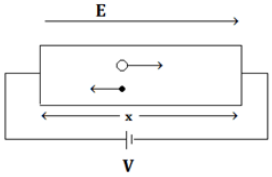
$$J = qD_n\left(\frac{d_n}{d_x}\right) amp/m^2$$
$$= 1.6\times10^{-19}\times0.0012\times1.5\times10^{22}$$
$$= 2.88 A/m^2$$

1.14 EINSTEIN'S RELATION

It states that, at thermal equilibrium, the ratio of diffusion constant to the mobility is constant. This is **Einstein's relation.** Mathematically it is expressed as,
$$\frac{Dp}{\mu_p} = \frac{Dn}{\mu_n} = kT = V_T$$
where, T is the temperature in $°K$
k is Boltzmann's constant
$= 8.62\times10^{-5} eV/°K$
V_T is called thermal voltage
$$V_T = \frac{T}{11600}$$
At $T=300^oK$,
$$V_T = \frac{300}{11600} = 0.0256V \approx 26mV$$

1.15 ELECTRIC FIELD

When a potential difference is applied across a material, a force acts on the charge carriers due to which electrons & holes move in the material i.e. a current flows through the material, this force on charge carriers is called electric field intensity.
Mathematically it is given by
$$E = -\frac{dV}{dx}\ V/m$$



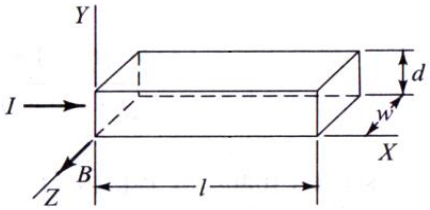
Note: In a material with uniform doping & uniform cross-sectional area the electric field is same at any point on the material

and the magnitude this electric field can be calculated using equation

$$E = \frac{\text{voltageapplied}}{\text{lengthofmaterial}}$$

1.16 HALL EFFECT

If specimen (metal or semiconductor) carrying a current I is placed in a transverse magnetic field B, an electric field *E* is induced in the direction perpendicular to both I and B. This phenomenon is known as the Hall Effect.



When a current carrying material is placed in transverse magnetic field, a force acts on the charge carriers called Lorentz's force given by

$$\vec{F} = q(v \times B)$$

where, q is charge of carriers(1.6×10^{-19}C)
v is velocity of charge carriers(m/s)
B is magnetic flux density (Tesla or weber/m^2)

The force acting on holes is $\overrightarrow{F_p} = +q(v_p \times B)$

For the given direction of current and magnetic field the direction of $(v_p \times B)$ is downward (direction of v_p is same as the direction of current) using right hand rule. Hence the direction of force on hole is also downward.

The force acting on electrons is

$$\overrightarrow{F_n} = -q(v_n \times B)$$

For the given direction of current and magnetic field the direction of $(v_n \times B)$ is upward (direction of v_n is opposite to that of current) using right hand rule. But as electrons are negatively charged carriers, the direction of force on electrons is also downward.

Due to displacement of charge carriers in the downward direction, a potential difference is developed across the top & bottom surfaces of the material called Hall voltage & mathematically its is given by

$$V_H = \frac{BI}{\rho w}$$

Where, ρ is called charge density

$$\rho = \frac{1}{\text{charge}(q) \times \text{carrierconcentration(norp)}}$$

The reciprocal of charge density is called hall coefficient.

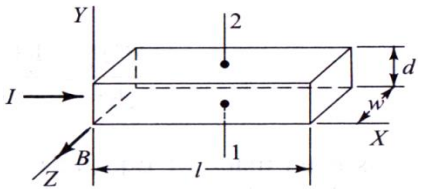
$$R_H = \frac{I}{\rho}$$

Applications:

1) It is used to determine whether a semiconductor is n-or p–type.
   (Type of material is determine by observing the polarity of hall voltage)
2) It is used to find the carrier concentration.
   (Carrier concentration (n or p) $= 1/(R_H \times q)$)
3) It is used to determine the mobility of charge carriers using equation $\mu = \sigma \times R_H$.
4) It is used to calculate magnetic flux density.

Example

Consider a rectangular cross –sectional semiconductor bar with lengthl = 12mm, width w = 5mm and thickness d = 4mm which is placed in the coordinate system as shown in fig. The positive and negative terminals of a battery of voltage $V_d = 5V$ are connected between the two cross–sectional surface of the bar at x = 0 and x = l respectively. A magnetic field $B = 6 \times 10^3$ Gauss is applied perpendicular to the bar along the +z-direction. If the bar is of n-type semiconductor with electron concentration $n_n = 2.5 \times 10^{15} cm^{-3}$and the current flowing through the bar is I = 10mA , determine the magnitude and polarity of the Hall voltage between the terminal 1 and 2. Also find the value of the Hall coefficient.



Solution

Since the semiconductor is of n-type with $n_n = 2.5\times10^{15}cm^{-3}$, the charge density ρ is given by

$$\rho \approx -qn_n = -\left(1.60\times10^{-19}C\right)\times2.5\times10^{15}cm^{-3}$$

$$= -4.0\times10^{-4}C/cm^3$$

The negative sign is used to denote that the type of majority carrier involved in the conduction of current in the semiconductor is electron.

Substituting the values of

$I = 10\times10^{-3}A$,

$$B = 6\times10^3 Gauss = \left(\frac{10^{-8}Wb}{cm^2}\right) = 6\times10^{-5}\frac{wb}{cm^2}$$

$\rho = 4.0\times10^{-4}C/cm^2$ and $w = 5\times10^{-1}cm$ in Eq; the magnitude of the Hall voltage is given by

$$V_H = \frac{BI}{\rho w} = 3.0\times10^{-3}V = 3.0mV$$

Since the direction of applied electric field is in the +X direction, the velocity of the electron v must be in the – X direction. Thus, the direction of deflection of the electrons can be determined as follows.

Let the magnetic field and velocity of electrons in the bar be expressed as

$$B = B\hat{z} \text{ and } v_e = -vx$$

Where $\hat{x}$ and $\hat{z}$ are the unit vectors along the +X and +Z directions. Thus the force acting on an electron is given by

$$F_e = e\left(B\times v_e\right) = eBv\left(-\hat{z}\times x\right) = eBv\left(-y\right)$$

Where $\hat{y}$ is the unit vector in the +Ydirection. Since the force is acting on the electron in the – y direction, the polarity of the Hall voltage at terminal 1 is negative with respective to the terminal 2.

Using Eq. the Hall coefficient can be obtained as

$$R_H = \frac{1}{\rho} = \frac{1}{4.0\times10^{-4}C/cm^{-3}} = -2.5\times10^3 cm^3/C$$

The negative sign in the value of Hall coefficient indicates that the sample used for Hall measurement is an n-type semiconductor.

1.17 PROPERTIES OF GERMANIUM & SILICON

Property	Ge	Si
Atomic number	32	14
Atoms per cm^3	4.42×10^{22}	5×10^{22}
E_{GO} at 0°K	0.785eV	1.21 eV
n_i at 300°K per cm^3	2.5×10^{13}	1.5×10^{10}
Intrinsic resistivity at 300°K in $\Omega-cm$	45	2.3×10^5
$\mu_n cm^2/V-sec$	3800	1300
$\mu_p cm^2/V-sec$	1800	500
$D_n cm^2/sec$	99	34
$D_p cm^2/sec$	47	13

GATE QUESTIONS

Q.1 n-type silicon is obtained by doping silicon with
a) Germanium b)Aluminum
c)Boron d)Phosphorous
[GATE-2003]

Q.2 The band gap of silicon at 300K is
a)1.36eV b)1.10 eV
c)0.80 eV d)0.67 eV
[GATE-2003]

Q.3 The intrinsic carrier concentration of silicon sample of 300K is 1.5 x $10^{16}/m^3$. If after doping, the number of majority carriers is $5x10^{20}/m^3$, the minority carrier density is
a) $4.50\times10^{11}/m^3$ b) $3.33\times10^{4}/m^3$
c) $5.00\times10^{20}/m^3$ d) $3.00\times\frac{10^{-5}}{m^3}$
[GATE-2003]

Q.4 The impurity commonly used for realizing the base region of a silicon n-p-n transistor is
a)Gallium b)Indium
c)Boron d)Phosphorus
[GATE-2004]

Q.5 The concentration of minority carriers in an extrinsic semiconductor under equilibrium is
a) Directly proportional to the doping concentration
b) Inversely proportional to the doping concentration
c) Directly proportional to the intrinsic concentration
d) Inversely proportional to the intrinsic concentration
[GATE-2006]

Q.6 Under low level injection assumption, the injected minority carrier current for an extrinsic semiconductor is essentially the
a) Diffusion current
b) Drift current
c) Recombination current
d) Induced current
[GATE-2006]

Q.7 The majority carriers in an n-type semiconductor have an average drift velocity V in a direction perpendicular to a uniform magnetic field B .The electric field E induced due to Hall effect acts in the direction
a) $V\times B$ b) $B\times V$
c) along V d)opposite to V
[GATE-2006]

Q.8 A heavily doped n-type semiconductor has the following data Hole-electron mobility ratio: 0.4 Doping concentration: 4.2×10^{8} atoms/m^3
Intrinsic concentration: 1.5×10^{4} atoms/m^3
The ratio of conductance of the n-type semiconductor to that of the intrinsic semiconductor of same material and at the same temperature is given by
a) 0.00005 b) 2,000
c) 10,000 d) 20,000
[GATE-2006]

Q.9 The electron and hole concentration in an intrinsic semiconductor are n_i per cm^3 at 300 K. Now, if acceptor impurities are introduced with a concentration of N_A per cm^3 (where N_A ? n_i),the electron concentration per cm^3 at 300 K will be
a) n_i b) $n_i + N_A$
c) $N_A - n_i$ d) $\frac{n_i^2}{N_a}$
[GATE-2007]

Q.10 Which of the following is true?

a) A silicon wafer heavily doped with boron is a p^+ substrate

b) A silicon wafer lightly doped with boron is a p^+ substrate

c) A silicon wafer heavily doped with arsenic is a p^+ substrate

d) A silicon wafer lightly doped with arsenic is a p^+ substrate

[GATE-2008]

Q.11 Silicon is doped with boron to a concentration of 4×10^{17} atoms / cm^3. Assume the intrinsic carrier concentration of silicon to be 1.5×10^{10} / cm^3 and the value of $\frac{kT}{q}$ to be 25 mV at 300 K. Compared to un doped silicon, the Fermi level of doped silicon.

a) goes down by 0.13 eV

b) goes up by 0.13 eV

c) goes down by 0.427 eV

d)goes up by 0.427 eV

[GATE-2008]

Q.12 In an n-type silicon crystal at room temperature, which of the following can have a concentration of $4\times10^{19}\,cm^{-3}$?

a)Silicon atoms

b)Holes

c)Dopant atoms

d)Valence electrons

[GATE-2009]

Q.13 The ratio mobility to the diffusion coefficient in a semiconductor has the units

a) V^{-1} b) $cm.V^{-1}$

c) $V.cm^{-1}$ d) V.s

[GATE-2009]

Q.14 Thin gate oxide in a CMOS process is preferably grown using

a) Wet oxidation

b) dry oxidation

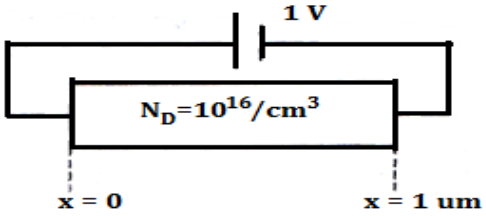
c) Epitaxial deposition

d) ion implantation

[GATE-2010]

Statement for Linked Answer Questions 15 & 16

The silicon sample with unit cross-sectional area shown below is in thermal equilibrium. The following information is given : T=300K, electronic charge $=1.6\times10^{-19}C$, thermal voltage =26 mV and electron mobility=1350 cm^2 / V – s



Q.15 The magnitude of the electric field at $x = 0.5\mu m$ is

a)1 kV/cm b) 5 kV/cm

c) 10kV/cm d) 26kV/cm

[GATE-2010]

Q.16 The magnitude of the electron drift current density at $x = 0.5\mu m$ is

a) $2.16\times10^4\,A/cm^2$

b) $1.08\times10^4\,A/cm^2$

c) $4.32\times\frac{10^3\,A}{cm^2}$

d) $6.48\times\frac{10^2\,A}{cm^2}$

[GATE-2010]

Q.17 Drift current in semiconductors depends upon

a) Only the electric field

b) Only the carrier concentration gradient

c) Both the electric field and the carrier concentration

d) Both the electric field and the carrier concentration gradient

[GATE-2011]

Q.18 In IC technology, dry oxidation (using dry oxygen) as compared to wet oxidation (using steam or water vapor) produces

a) Superior quality oxide with a higher growth rate
b) Inferior quality oxide with a higher growth rate
c) Inferior quality oxide with a lower growth rate
d) Superior quality oxide with a lower growth rate

[GATE-2013]

Q.19 The doping concentrations on the p-side and n-side of a silicon diode are $1\times 10^{16}cm^{-3}$ and $1 \times 10^{17}cm^{-}$, respectively. A forward bias of 0.3 V is applied to the diode. At T = 300K, the intrinsic carrier concentration of silicon n_i =1.5×10^{10} cm^{-3} and $\frac{kT}{q}$= 26mV. The electron Concentration at the edge of the depletion region on the p-side is

a) $2.3 \times 10^{9}cm^{-3}$ b) $1 \times10^{16}cm^{-3}$
c) $1 \times10^{17}cm^{-3}$ d) $2.25 \times 10^{6}cm^{-3}$

[GATE-2014]

Q.20 A silicon bar is doped with donor impurities N_D =$2.25x10^{15}$ atoms/ $cm^{3.}$ Given the intrinsic carrier concentration of silicon at T = 300 K is n_i = 1.5×10^{10} cm^{-3}. Assuming complete impurity ionization, the equilibrium electron and hole concentrations are

a) $n_0=1.5x10^{16}$ cm^{-3}, $po=1.5x10^{5}$ cm^{-3}

b) $n_0=1.5x10^{10}cm^{-3,}$ $po=1.5x10^{15}cm^{-3}$

c)$n_0=2.25x10^{15}cm^{-3}$,$po=1.5x10^{10}cm^{-3}$

d) $n_0=2.25x10^{15}$ cm^{-3}, $po=1x10^{5}cm^{-3}$

[GATE-2014]

Q.21 Assume electronic charge q = $1.6x10^{-19}C$, kT/q = 25 mV and electron mobility μ_n. = 1000 cm^2/V-s. If the concentration gradient of electrons injected into a P-type silicon sample is $1x10^{21}/cm^4$, the magnitude of electron diffusion current density (in A/cm^2) is_____.

[GATE-2014]

Q22 When a silicon diode having a doping concentration of N_A= 9 x 10^{16} cm^{-3} on p-side and N_D= 1 x 10^{16} cm^{-3} on n-side is reverse biased, the total depletion width is found to be 3 μm Given that the permittivity of silicon is 1.04 x 10^{-12} F/cm, the depletion width on the p-side and the maximum electric field in the depletion region, respectively, are

a) 2.7 μm and 2.3 x 10^5 V/cm
b) 0.3µm and 4.15 x 10^5 V/cm
c) 0.3µm and 0.42 x 10^5 V/cm
d) 2.1 µm and 0.42 x 10^5 V/cm

[GATE-2014]

Q.23 A thin P-type silicon sample is uniformly illuminated with light which generates excess carriers. The recombination rate is directly proportional to

a) The minority carrier mobility
b) The minority carrier recombination lifetime
c) The majority carrier concentration
d) The excess minority carrier concentration

[GATE-2014]

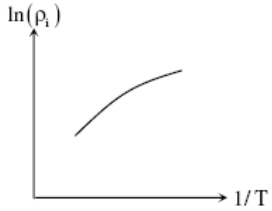
Q.24 At T = 300 K, the band gap and the intrinsic carrier concentration of GaAs are 1.42 eV and 10^6 cm^{-3}, respectively. In order to generate electron hole pairs in GaAs, which one of the wavelength (λ_c) ranges of incident radiation, is most suitable? (Given that: Plank's constant is 6.62 x 10^{-34} J-s, velocity of light is 3×10^{10} cm/s and charge of electron is 1.6 x 10^{-19}C)

a) 0.42 µm < λ_c < 0.87 µm
b) 0.87 µm < λ_c < 1.42 µm

c) 1.42 μm < λ_c < 1.62 μm
d) 1.62 μm < λ_c < 6.62 μm

[GATE-2014]

Q.25 In the figure $\ln(\rho_i)$ is plotted as a function of 1/T, where ρ_i the intrinsic resistivity of silicon, T is the temperature, and the plot is almost linear.



The slope of the line can be used to estimate

a) Band gap energy of silicon (Eg)
b) Sum of electron and hole mobility in silicon ($\mu_n + \mu_p$)
c) Reciprocal of the sum of electron and hole mobility in silicon ($\mu_n + \mu_p)^{-1}$
d) Intrinsic carrier concentration of silicon (n_i)

[GATE-2014]

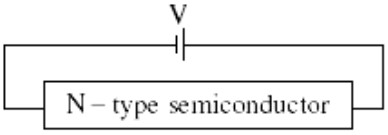
Q.26 The cut-off wavelength (in μm) of light that can be used for intrinsic excitation of a semiconductor material of bandgap Eg= 1.1 eV is_____.

[GATE-2014-4]

Q.27 Consider a silicon sample doped with N_D = 1x10^{15}/cm^3 donor atoms. Assume that the intrinsic carrier concentration n_i=1.5x10^{10}/cm^3. If the sample is additionally doped with NA = 1x10^{18}/cm^3 acceptor atoms, the approximate number of electrons/cm^3 in the sample, at T=300 K, will be _____.

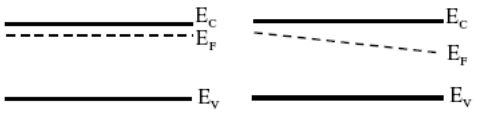
[GATE-14-4]

Q.28 An N-type semiconductor having uniform doping is biased as shown in the figure.

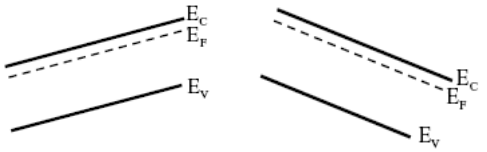


If E_c is the lowest energy level of the conduction band, E_v is the highest energy level of the valance band and E_F is the Fermi level, which one of the following represents the energy band diagram for the biased N-type semiconductor?

a) b)



c) d)

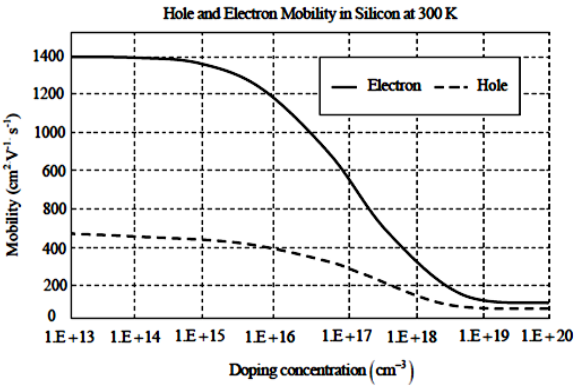


[GATE-2014-4]

Q.29 A silicon sample is uniformly doped with donor type impurities with a concentration of $10^{16}/cm^3$. The electron and hole mobilities in the sample are 1200 cm^2 / V– s and 400cm^2/V–s respectively. Assume complete ionization of impurities. The charge of an electron is 1.6 $\times 10^{-19}$ C. The resistivity of the sample (in Ω– cm) is _____.

[GATE-2015-1]

Q.30 A piece of silicon is doped uniformly with phosphorous with a doping concentration of $10^{16}/cm^3$. The expected value of mobility versus doping concentration for silicon assuming full dopant ionization is shown below. The charge of an electron is 1.6×10^{-19} C. The conductivity (in S cm^{-1}) of the silicon sample at 300 K is _____.

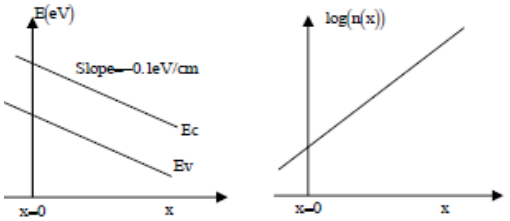


[GATE-2015-2]

Q.31 An n+type silicon sample is uniformly illuminated with light which generates 1020 electron hole pairs per cm3 per second. The minority carrier lifetime in the sample is 111,s . Int eh steady state, the hole concentration in the sample is approximately 10' , where x is an integer. The value of x is

[GATE-2015-2]

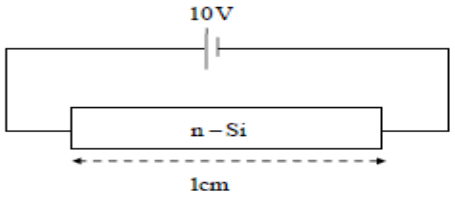
Q.32 The energy band diagram and electron density profile n(x) in a semiconductor are shown in the figure. Assume that $n(x)= 10^{15} e^{\left(\frac{qax}{kT}\right)} cm^{-3}$, with $\alpha = 0.1V / cm$ and x expressed in cm. Given $\frac{kT}{q} = 0.026V$, $D_n = 36\ cm^2 s^{-1}$,& $\frac{D}{\mu} = \frac{kT}{q}$. The electron current density (in A / cm^2) at x = 0 is



a) -4.4×10^{-2}
b) -2.2×10^{-2}
c) 0
d) 2.2×10^{-2}

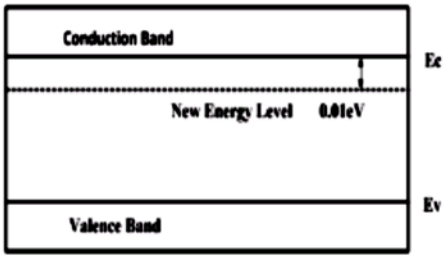
[GATE-2015-2]

Q.33 A dc voltage of 10V is applied across an n-type silicon bar having a rectangular cross-section & a length of l cm as shown in figure. The donor doping concentration N_D and the mobility of electrons μ_n are $10^{16} cm^{-3}$ & 1000 $cm^2\ V^{-1} s^{-1}$, respectively . The average time (in μs) taken by the electrons to move from one end of the bar to other end is _____.



[GATE-2015-2]

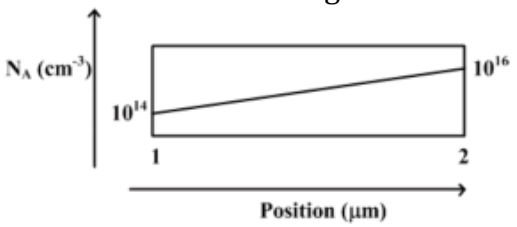
Q.34 A small percentage of impurity is added to an intrinsic semiconductor at 300 K. Which one of the following statements is true for the energy band diagram shown in the following figure?



a) Intrinsic semiconductor doped with pentavalent atoms to form n-type semiconductor
b) Intrinsic semiconductor doped with trivalent atoms to form n-type semiconductor
c) Intrinsic semiconductor doped with pentavalent atoms to form p-type semiconductor
d) Intrinsic semiconductor doped with trivalent atoms to form p-type semiconductor

[GATE-16-1]

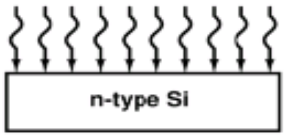
Q.35 The figure below shows the doping distribution in a p-type semiconductor in log scale.



The magnitude of the electric field (in kV/cm) in the semiconductor due to non uniform doping is _____.

[GATE-16-1]

Q.36 Consider a silicon sample at T=300K, with a uniform donor density $N_d = 5\times10^{16}\,cm^{-3}$ illuminated uniformly such that the optical generation rate is $G_{opt} = 1.5\times10^{20}\,cm^{-3}s^{-1}$ throughout the sample. The incident radiation is turned off at t=0. Assume low-level injection to be valid and ignore surface effects. The carrier lifetimes are τ_{p0} = 0.1 μs and τ_{n0} = 0.5μs



The hole concentration at t = 0 and the hole concentration at t =0.3 μs, respectively, are

a) $1.5\times10^{13}\,cm^{-3}$ & $7.47\times10^{11}\,cm^{-3}$

b) $1.5\times10^{13}\,cm^{-3}$ & $8.23\times10^{11}\,cm^{-3}$

c) $7.5\times10^{13}\,cm^{-3}$ & $3.73\times10^{11}\,cm^{-3}$

d) $7.5\times10^{13}\,cm^{-3}$ & $4.12\times10^{11}\,cm^{-3}$

[GATE-2016-1]

Q.37 A bar of Gallium Arsenide (GaAs) is doped with Silicon such that the Silicon atoms occupy Gallium and Arsenic sites in the GaAs crystal. Which one of the following statement is true?

a) Silicon atoms act as p-type dopants in Arsenic sites and n-type dopants in Gallium sites

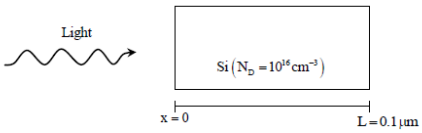
b) Silicon atoms act as n-type dopants in Arsenic sites and p-type dopants in Gallium sites

c) Silicon atoms act as p-type dopants in Arsenic as well as Gallium sites

d) Silicon atoms act as n-type dopants in Arsenic as well as Gallium sites

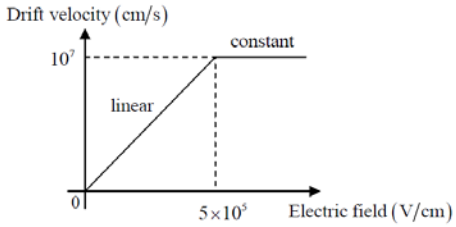
[GATE-2017-1]

Q.38 As shown a uniformly doped Silicon (Si) bar of length L = 0.1 with a donor concentration $N_D = 10^{16}cm^{-3}$ is illuminated at x = 0 such that electron and hole pairs are generated at the rate of $G_L = G_{L0}\left(1-\frac{x}{L}\right), 0 \le x \le L$ where $G_{L0} = 10^{17}cm^{-3}s^{-1}$. Hole lifetime is 10^{-4}s, electronic charge q = 1.6 x 10^{-19}C , hole diffusion coefficient $D_P = 100cm^2/s$ and low level injection condition prevails. Assuming a linearly decaying steady state excess hole concentration that goes to 0 at x = L, the magnitude of the diffusion current density at x = L/2, in A/cm^2 is _____. m



[GATE-2017-1]

Q.39 The dependence of drift velocity of electrons on electric field in a semiconductor is shown below. The semiconductor has a uniform electron concentration of n = 1 x $10^{16}cm^{-3}$ and electronic charge q = 1.6 x 10^{-19}C. If a bias of 5V is applied across a 1 region of this semiconductor, the resulting current density in this region, in kA/cm^2, is _____.



[GATE-2017-1]

Q.40 A junction is made between p- Si with doping density $N_{A1} = 10^{15}$ cm^{-3} and p Si with doping density $N_{A2} = 10^{17}$cm^{-3}

Given: Boltzmann constant k = 1.38 × 10^{-23} J.K^{-1}, electronic charge

q = 1.6 × 10^{-19} C. Assign 100% acceptor ionization. At room temperature (T = 300 K), the magnitude of the built-in potential (in volts, correct to two decimal places) across this junction will be____.

[GATE-2018]

ANSWER KEY:

1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
(d)	(b)	(a)	(c)	(b)	(a)	(b)	(d)	(d)	(a)	(c)	(c)	(a)	(b)
15	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**	**26**	**27**	**28**
(c)	(a)	(c)	(d)	(a)	(d)	4000	(b)	(d)	(a)	(a)	225.2	(d)	0.52
29	**30**	**31**	**32**	**33**	**34**	**35**	**36**	**37**	**38**	**39**	**40**		
1.92	14	(c)	100	(a)	(a)	(a)	(a)	(a)	16	1.6	0.1192		

EXPLANATIONS

Q.1 (d)

N-type silicon is obtained by doping silicon with a pentavalent impurity i.e. phosphorus.

Q.2 (b)

Q.3 (a)

$n_i^2 = np$

n_i = intrinsic concentration

$$p = \frac{n_i^2}{n} = \frac{1.5\times10^{16}\times1..5\times10^{16}}{5\times10^{20}}$$

$$= 45\times10^{10} = 4.5\times10^{11}$$

Q.4 (c)

For an n-p-n transistor, the base region is a p type semiconductor. In the options there are 3 trivalent impurities but for silicon boron is preferred.

Q.5 (b)

Minority concentration

$$= \frac{n_i^2}{\text{majority carrier concentration}}$$

$$I, e, p \propto \frac{1}{h}$$

Q.6 (a)

The injected minority carrier current is diffusion current and it is because of concentration gradient.

Q.7 (b)

The electric field will be perpendicular to both V and B, and inB × V direction.

Q.8 (d)

$$\frac{\sigma_n}{\sigma_i} = \frac{nq\mu n}{n_i q(\mu_n + \mu_p)} = \frac{n}{n_i\left(1+\frac{\mu_p}{\mu_n}\right)}$$

$$= \frac{4.2\times10^8}{1.5\times10^{4[1+0.4]}} = 20,000$$

Q.9 (d)

By the law of electrical neutrality

$p + N_D = n + N_A$

As $N_D = 0$

N_A ? $n_i \cong 0 p = N_A$

Using mass action law np= n_i^2

So, $n = \frac{n_i^2}{p} = \frac{n_i^2}{N_A}$

Q.10 (a)

Boron is acceptor impurity, so high concentration makes p^+substrate.

Q.11 (c)

For p-type material ,

$N_A = n_i e^{+(E_{Fi}-E_F)/KT}$

$\Rightarrow 4\times10^{17} = 1.5\times10^{10} e^{(E_{Fi}-E_F)/KT}$

$\Rightarrow \frac{E_{Fi}-E_F}{KT} = 17.1$

$\Rightarrow E_{Fi} - E_F = 17.1\times 25mv$

$= 0.427eV$

It is p-type so Fermi level goes down by 0.427eV

Q.12 (c)

Q.13 (a)

$$\frac{D}{\mu} = V_T$$

$$\Rightarrow \frac{\mu}{D} = \frac{1}{V_T} \Rightarrow \text{units} : V^{-1}$$

Q.14 (b)

Dry oxidation is preferred because of less contamination.

Q.15 (c)

Electric field will be constant inside sample.

$$E = \frac{V}{d} = \frac{1}{10^{-6}} = 10kV/cm$$

Q.16 (a)

$$J = n\mu_n q\varepsilon$$
$$= 10^{16} \times 1350 \times 1.6 \times 10^{-19} \times 10 \times 10^3$$
$$= 2.16 \times 10^4 A/cm^2$$

Q.17 (c)

$J = n\, e V_d$

Put, $V_d = \mu E$

$\therefore \quad J = n\, e\, \mu E$

Hence, $I = n\, e\, \mu\, EA$

So, it depends upon carrier concentration and electric field

Q.18 (d)

The designed characteristics and requirements of the fabricated oxide can be mainly influenced by the used oxidant species. With dry oxidation, normally high –quality thin oxide films are produced. During wet oxidation, the silicon water is settled to a water vapor temperature .Wet oxide grow really fast compared to any oxidation, which is the biggest advantage.

Q.19 (a)

Electron concentration,

$$n = \frac{n_i^2}{N_A} e^{V_{bi}/V_T}$$
$$= \frac{(1.5 \times 10^{10})^2}{1 \times 10^{16}} e^{0.3/26mV}$$
$= 2.3 \times 10^9 / cm^3$

Q.20 (d)

$N_D = 2.25 \times 10^{15}$ Atom / cm^3

$h_i = 1.5 \times 10^{10} / cm^3$

Since complete ionization taken place,

$h_0 = N_D = 2.25 \times 10^{15} / cm^3$

$$P_0 = \frac{n_i^2}{n_0} = \frac{(1.5 \times 10^{10})^2}{2.25 \times 10^{15}} = 1 \times 10^5 / cm^3$$

Q.21 (4000)

Given q $= 1.6 \times 10^{-19}$; $-\frac{KJ}{q} = 2.5$ mV, μ_n.

$= 1000\ cm^2 / v - s$

From Einstein relation, $\frac{D_n}{\mu_n} = \frac{KJ}{q}$

$\Rightarrow D_n = 25mV \times 1000 cm^2 / v - S$

$\Rightarrow 25\ cm^2 / s$

Diffuion current Density $J = qD_n \frac{dn}{dx}$

$= 1.6 \times 10^{-19} \times 25 \times 1 \times 10^{21}$

$= 4000A / cm2$

Q.22 (b)

Given $N_A = 9 \times 10^{16} / cm^3$; $N_D = 1 \times 10^{16} / cm^3$

Total depletion width $x = x_n + x_p = 3\mu m$

$\epsilon = 1.04 \times 10^{-12} F / cm$

$\frac{x_n}{x_p} = \frac{N_A}{N_D} = \frac{9 \times 10^{16}}{1 \times 10^{16}}$

$x_n = 9\, x_p$ .....(1)

Total Depletion width, $x_n + x_p = 3\ \mu m$

$9\, x_p + x_p = 3\ \mu m$

$x_p = 0.3\mu m$

Max. Electric field, E =

$$\frac{qN_A X_p}{\epsilon} = \frac{1.6 \times 10^{-19} \times 9 \times 10^{16} \times 0.3\mu m}{1.04 \times 10^{-12}}$$
$= 4.15 \times 10^5 V/cm$

Q.23 (d)

Recombination rate,

$$R = B(n_{n_o} + n_n')\left(P_{n_o} + P_n'\right)$$

n_{no} & P_{no} = Electron and hole concentrations respectively under thermal equilibrium

n_n' & P_n' = Excess elements and hole concentrations respectively

Q.24 (a)

$$E = \frac{hc}{\lambda} \Rightarrow \lambda = \frac{6.62 \times 10^{-34} \times 3 \times 10^8}{1.42 \times 1.6 \times 10^{-19}} = 0.87\mu m$$

Q.25 (a)

$n_i \alpha T^{3/2} e^{-Eg/kT}$ and $\rho_i \alpha \frac{1}{\eta_i}$

$\therefore$ From the graph, Energy graph of S_i can be estimated

Q.26 (225.2)

P=N_A-N_D=1x10^{18}–1x10^{15}=9.99 x10^{17}

$$\eta = \frac{\eta_i^2}{P} = \frac{(1.5\times10^{10})^2}{9.99\times10^{17}} = 225.2/cm^3$$

Q.27 (d)

Q.28 (0.52)

$$P = \frac{1}{\sigma_N} = \frac{1}{N_D q \mu_n}$$

$$= \frac{1}{10^{16}\times1.6\times10^{-19}\times1200}$$

= 0.52Ω-cm

Q.29 (1.92)

As per the graph mobility of electrons at the concentration $10^{16}/cm^3$is 1200 $\frac{cm^2}{V-s}$

So, μ_n =1200 $\frac{cm^2}{V-s}$

$\sigma_n = N_D q \mu_n$

$= 10^{16}\times1.6\times10^{-19}\times1200$

$= 1.92\ S\ cm^{-1}$

Q.30 (14)

The concentration of hole-electron pair in lvt sec =1020 x 10-6 = 1014/cm3 So, the power of 10 is 14. x =14

Q.31 (c)

$$J_n\ (diff) = qD_n \frac{dn(x)}{dx}$$

Given $n(x) = 10^{15}e^{\frac{qax}{kT}}$

$$\left.\frac{d_n(x)}{dx}\right|_{x=0} = 3.846\times10^{15}\ cm^4$$

$$J_n(diff) = 2.2\times10^{-2}\ A/cm^2$$

$$\left.J_{n(drift)}\right|_{x=0} = n(0).q\mu_n E_x$$

$$= 10^{15}\times1.6\times10^{-19}\times1384.5\times E_x$$

$$E_x = \frac{-kT}{q}.\frac{1}{n(x)}.\frac{d_n(x)}{dx}$$

= -α = -0.1 V/cm

$J_{n(drift)}$= -2.2× 10^{-12} A/cm^2

$$J = J_{n(drift)} + J_{n(drift)} = 0A/cm^2$$

Q.32 (100)

$$\varepsilon = \frac{V}{d} = \frac{10}{1} = 10V/m$$

$$V_d = \mu\varepsilon = 1000\times10 = 10^4 cm/s$$

$$V_d = \frac{L}{T} \Rightarrow T = \frac{L}{V_d} = \frac{1\times100}{10^4\times10^2} = 100\mu s$$

Q.33 (a)

New energy level is near to conduction band, so it is pentavalent atoms to form n-type semiconductor.

Q.34 (1.10 to 1.25)

Q.35 (a)

$$P_{n0} = \frac{n_i^2}{N_D} = \frac{2.25\times10^{20}}{5\times10^{16}} = 0.5\times10^4/cc$$

$$\rightarrow \Delta P = G\tau_{p0} = 1.5\times10^{20}\times10^{-6}\times0.1 = 1.5\times10^3/cc$$

$$\Delta P(t) = \Delta p e^{-t/\tau_p}$$

$$P(t) = \Delta P(t) + P_{n0} \approx \Delta P(t)$$

$$\Delta P(0) = \Delta P = 1.5\times10^{13}/cc$$

$$\Delta P(t=3) = 7.47\times10^{11}/cc$$

Q.36 (a)

Given

$$G_{opt} = 1.5x10^{20}/cm^3/sec$$

$$G_{opt} = R = \frac{N_A}{\tau_p}$$

$$1.5x10^2 = \frac{N_A}{0.1x10^{-6}}$$

$$N_A = 1.5x10^{13}/cm^3$$

$$P(t) = P_{n0}e^{-t/\tau_p}$$

$$= 1.5x10^{13}e^{\frac{-0.3}{0.1}}$$

$$= 7.46x10^{11}/cm^3$$

Q.37 (a)

Silicon atoms act as P- type dopants in Arsenic sites and n- type dopants in Gallium sites.

Q.38 15.9-16.1

$$\Delta P = \Delta n = G_{L0}\left(1-\frac{\frac{L}{2}}{L}\right)\tau_p$$

$$= G_{L0} x \frac{1}{2}\tau_p$$

$$= 10^{17} x \frac{1}{2} x 10^{-4}$$

$$= \frac{1}{2} x 10^{13} / cm^3$$

$$\left|J_{P_i} diff\right| = qD_P \frac{dp}{dx}$$

$$= 1.6x10^{-19} x100 \frac{\frac{1}{2}x10^{13}}{\frac{0.1x10^{-4}}{2}}$$

$$= 16A / cm^2$$

Q.39 1.5-1.7

$$v_d = \mu_n \varepsilon$$

$$\mu_n = \frac{v_d}{\varepsilon} = \frac{10^7}{5x10^5} 20 \frac{cm^2}{v-sec}$$

$$E = \frac{V}{d} = \frac{5}{1x10^{-4}} V / cm$$

$$J_{drift} = nqv_d = nq\mu_n\varepsilon$$

$$J_{drif}t = nqv_a = nq\mu_n\varepsilon$$

$$= 10^{16} x1.6x10^{-19} x20x5x10^4 = 1.6kA / cm^2$$

Q.40 0.1192

Setting $J_p = 0$

$$E = \frac{V_T}{P}\frac{dP}{dx}$$

$$dV = -V_T \frac{dP}{dx}\left[E = -\frac{dV}{dx}\right]$$

$$V_{21} = V_2 - V_1 = V_T \ln\left(\frac{P_1}{P_2}\right)$$

Built in potential

$$V_{bi} = \frac{kT}{q}\ln\left(\frac{N_{A2}}{N_{A1}}\right)$$

$$= \frac{1.38x3}{1.6x100}\ln(100)V$$

$$= 0.1192V$$

2 P-N JUNCTION DIODES

2.1 JUNCTION THEORY

PN junction is formed in a single crystal of semiconductor by making one end of the crystal p-type by doping it with acceptor atom and making the other end n-type by doping with donor atoms. The region where p-type and n-type meet is the junction.

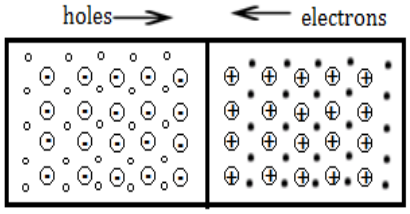


fig. 1

When two semiconductor material types, p-type and n-type are brought to contact, majority carrier of each type would diffuse across the junction i.e. the majority carrier hole from p-type diffuses to n-type material and the majority carrier electron from n-type diffuses to p-type material.

As the majority carrier such as hole diffuses across the junction, it combines with electron in the n-type side, which creates a net positive charge. Likewise, the majority carrier electron from n-type material diffuses across the junction recombines with hole in p-type side creates net negative charge. The net charge at each side creates an electric field in the direction from N type to P type semiconductor, which would oppose further diffusion of majority charge carriers. The electric field created would drift the minority carrier in the opposite direction across the junction. Thus when equilibrium attained, the drift carriers and diffused carriers should be balanced in terms of magnitude and in opposite direction.

As the result of this process, a depletion region i.e. a region of lack of carrier of certain thickness is created on both sides of the junction. The depletion region is also termed as space charge region.

Figure 1: shows majority carrier diffusion in pn junction

Figure 2: A pn junction showing depletion region

Figure 3: Charge density on either sides of the junction

Figure 4: Electric field across the depletion layer

Figure 5: Potential barriers

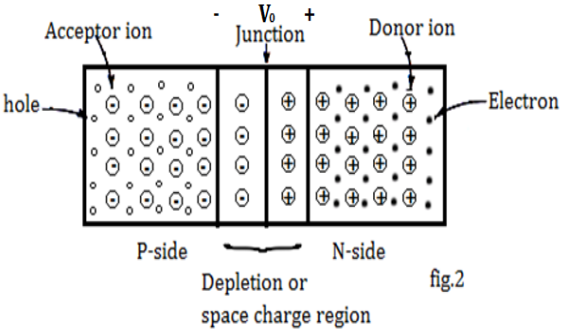


fig.2

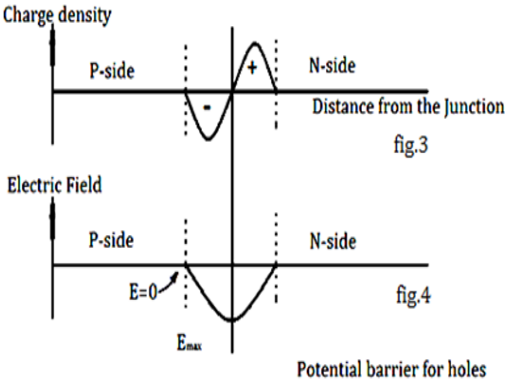


fig.3

fig.4

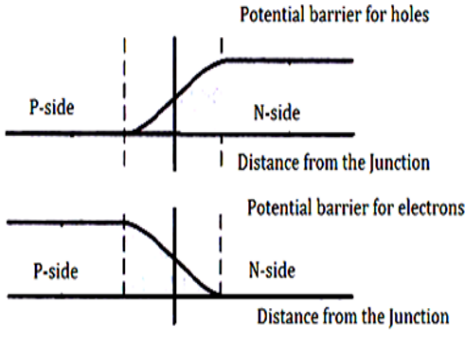


fig.5

Due to positive & negative charges on either sides of depletion layer a potential is developed across the depletion layer called as contact potential (V_o) or built-in

potential (V_{bi}) or junction potential (V_j). Magnitude of this contact potential depends on temperature & doping on P & N sides

$$V_0 = V_T \ln \ln \left(\frac{N_A N_D}{n_i^2} \right) \text{volts}$$

Where,

V_T is thermal voltage

$V_T \approx 26\text{mV at } T = 300^\circ K$

N_A is doping on N – side

N_D is doping on P – side

n_i is intrinsic carrier concentration

$n_i = 2.5 \times 10^{13} \text{ atoms/cm}^3$

for germanium

$n_i = 1.5 \times 10^{10} \text{ atoms/cm}^3$

for silicon

The width of depletion layer formed near the junction is of the order of $10^{-6}\text{m} = 1\text{micron}$ & is mathematically given by

$$W = \sqrt{\frac{2\varepsilon}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right) V_O}$$

Where, $\varepsilon = \varepsilon_o \varepsilon_r$

ε_o is permitivity of free space

$\varepsilon_o = 8.85 \times 10^{-12} \text{ F/m}$

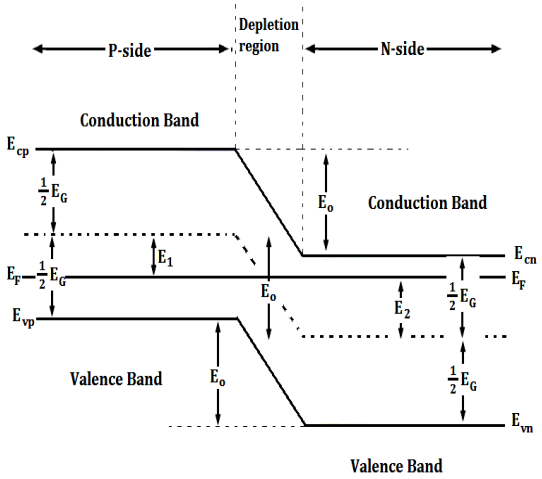
$\varepsilon_o = 8.85 \times 10^{-14} \text{ F/cm}$

ε_r is relative permitivity of the material

Note: The magnitude of the electric field induced across the junction is maximum at the junction.

2.1.1 BAND STRUCTURE OF OPEN CIRCUITED PN JUNCTION

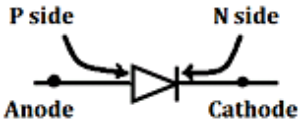
When a PN junction is formed the Fermi level must be same throughout the diode. If this were not so, electrons on one side of the junction would have an average energy higher than those on the other side, and there would be a transfer of electrons and energy until the Fermi levels in the two sides did line up.



The Fermi level E_F is closer to the conduction band edge E_{Cn} in the N-type material (like in isolated N-type SC) and closer to the valence band edge E_{Vp} in the p side (like in isolated P-type SC). Clearly, then the conduction band edge E_{Cp} in the p material cannot be at the same level as E_{Cn}, nor can the valence band edge E_{Vn} in the n side line up with E_{Vp}. Hence the energy–band diagram for a p-n junction appears as shown in Fig. where a shift in energy level E_o is indicated. Note that

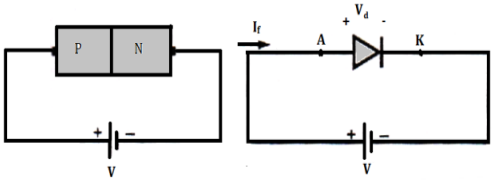
$E_o = E_{Cp} - E_{Cn} = E_{Vp} - E_{Vn} = E_1 + E_2$

2.1.2 CIRCUIT SYMBOL



2.2 PN JUNCTION IN FORWARD BIAS

When anode terminal of diode is biased at higher potential with respect to cathode terminal (or positive terminal of battery connected to P-side & negative terminal connected to N-side), a PN junction diode is said to be forward biased.



When PN junction is forward biased the effect of electric field across the depletion layer decreases on majority charge i.e. the height of potential barrier decreases & majority charge carriers are injected to the other sides of diode i.e. holes are injected from P to N while electrons are injected from N to P. These carriers move away from the junction due to diffusion and will eventually recombine with majority carriers of other region. Due to the applied forward voltage the minority charge carriers move away from the junction i.e. they do not take part in conduction.

The forward current of diode I_f is related to the voltage V_d by the equation

$$I_f = I_0 \lfloor \exp(V_d / \eta V_T) - 1 \rfloor$$

Where, I_0 is reverse saturation current

V_d is forward voltage across diode

$\eta = 1$ for germanium

$\eta = 2$ for silicon

V_T is thermal voltage

$$V_T = \frac{T}{11,600} = 26\text{mV at } T = 300°K$$

As, $\exp(V_d / \eta V_T) \gg 1$

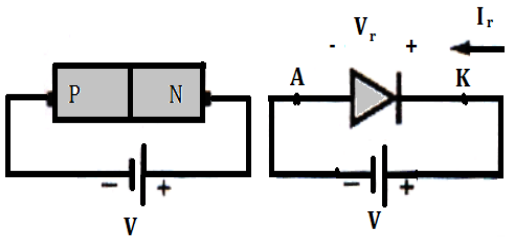
$\therefore I_f = I_0 \exp(V_d / \eta V_T)$

Note:

1) The direction of I_f is from P-side to N-side.
2) The width of depletion layer decreases with the increase in applied forward voltage.
3) The forward current is basically diffusion current.

2.3 PN JUNCTION IN REVERSE BIAS

When cathode terminal of diode is biased at higher potential with respect to anode terminal (or positive terminal of battery connected to N-side & negative terminal connected to P-side), a PN junction diode is said to be reverse biase



When PN junction is reversed biased the majority charge carriers cross the junction while majority charge carriers move away from the junction. The reverse current in the diode flows due to minority charge carriers & it is called as reverse saturation current, minority carrier current, leakage current or thermally generated current.

$$I_r = I_0 \lfloor \exp(-V_r / \eta V_T) - 1 \rfloor$$

Normally, $\exp(-V_r / \eta V_T) \ll 1$

$\therefore I \approx -I_0$ thus the reverse current is constant & independent of the applied reverse bias.

In a reverse biased PN junction, the depletion layer width is given by

$$W = \sqrt{\frac{2\varepsilon}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)(V_O + V_r)}$$

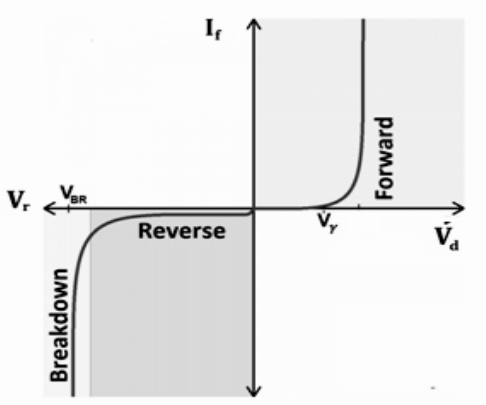
i.e. $W \propto \sqrt{(V_O + V_r)}$

Hence, the width of depletion layer in diode increases with applied reverse voltage.

Note:

1) The direction of reverse current is from N-side to P-side.
2) The reverse current is basically drift current.

2.4 I-V CHARACTERISTICS



1) In a forward biased PN junction the current through diode increases exponentially with applied forward voltage.
2) In a reverse biased PN junction is of the order of neon amperes for silicon & micro amperes for germanium.

2.4.1 CUT-IN VOLTAGE (V_γ)

It is the minimum value of V_d for which diode enters into conduction when it is forward biased. Below V_γ the current through diode is negligibly small.

$V_\gamma \approx 0.2V$ for germanium diode

$V_\gamma \approx 0.7V$ for silicon diode

2.4.2 DIODE RESISTANCE

For small –signal operation the dynamic, or incremental, resistance r is defined as the reciprocal of the slope of the volt –ampere characteristic.

$$r = \frac{dV_d}{dI_f}$$

$$r \approx \frac{\eta V_T}{I_f}$$

Note: The dynamic resistance of diode is not constant; it decreases exponentially with applied forward voltage.

2.4.3 DYNAMIC CONDUCTANCE

The dynamic conductance is the slope of volt-ampere characteristics of diode.

$$g = \frac{1}{r}$$

$$g = \frac{dI_f}{dV_d}$$

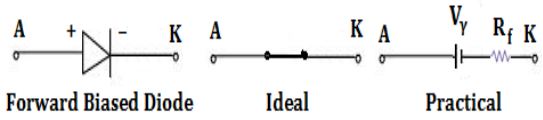
$$= \frac{I_0 \exp\left(\frac{V_d}{\eta V_T}\right)}{\eta V_T}$$

$$= \frac{I_f + I_0}{\eta V_T} \approx \frac{I_f}{\eta V_T}$$

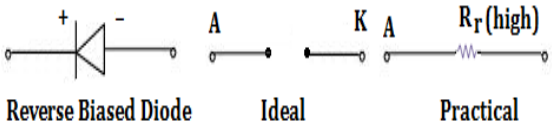
Note: The dynamic conductance of diode is not constant, it increases exponentially with applied forward voltage.

2.4.4 EQUIVALENT CIRCUITS

1) Forward Bias: An ideal diode in forward bias can be replaced with short circuit & a practical diode can be replaced with a battery (cut-in voltage) & a series resistance (if given).



2) Reverse Bias: An ideal diode in reverse bias can be replaced by an open circuit & a practical diode can be replaced with a reverse resistance (if given).



2.5 EFFECT OF TEMPERATURE

1) REVERSE SATURATION CURRENT (I_0): It increases approximately 7 percent per ℃ rise in temperature for both silicon and germanium & it approximately doubles for every 10℃ rise in temperature.

$$I_{0T_2} = I_{0T_1} \times 2^{\left(\frac{T_2 - T_1}{10}\right)}$$

where, I_{0T_2} is reverse saturation current at temperature T_2

I_{0T_1} is reverse saturation current at temperature T_1

2) FORWARD VOLTAGE ACROSS DIODE (V_d): Forward voltage of diode decreases with temperature

$$\frac{dV_d}{dT} = \begin{cases} -2.1mV/℃ \text{ for Ge} \\ -2.3mV/℃ \text{ for Si} \end{cases}$$

In general, the temperature coefficient of V_d is considered as $2.5mV/℃$

i.e. $\frac{dV_d}{dT} = -2.5mV/℃$

2.6 DIODE CAPACITANCES

Any variation of the charge within a p-n diode with an applied voltage variation yields a capacitance which must be added to the circuit model of a p-n diode. The capacitance associated with the charge variation in the depletion layer is called the **junction capacitance or transition capacitance or depletion capacitance**, while the capacitance associated with the excess carriers in the quasi-neutral region is called the **diffusion capacitance**. Both types of capacitance are present in the forward- and reverse-bias regions, but one dominates the other in each region that we consider the effect of only one in each region.

2.6.1 TRANSITION CAPACITANCE

A reverse bias causes majority carriers to move away from the junction hence the thickness of the space–charge layer at the junction increases with reverse voltage, thereby uncovering more immobile charges. This increase in uncovered charge with applied voltage may be considered a capacitive effect. We may define an incremental capacitance C_T as

$$C_T = \left|\frac{dQ}{dV}\right|$$

The quantity C_T is referred to as the transition, space–charge, barrier or depletion region capacitance.

$$C_T = \frac{\varepsilon A}{W}$$

where, W is depletion region width

$$W = \sqrt{\left\{\frac{2\in}{e}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)\right\}(V_o + V_r)}$$

$\varepsilon = \varepsilon_0\varepsilon_r$

A is cross sectional area of diode

As $W \propto \sqrt{(V_O + V_r)}$, the transition capacitance

$$C_T \propto \frac{1}{\sqrt{(V_O + V_r)}} v$$

Note: In general $C_T \propto \frac{1}{(V_r)^m}$

Where $m = \frac{1}{2}$ for step graded PN junction

$m = \frac{1}{3}$ for linearly graded PN junction

$m = \frac{1}{2.5}$ for diffused PN junction

When no reverse voltage is applied i.e. $V_r = 0V$ then the capacitance is C_{T0}.

$$C_T = \frac{C_{T0}}{\sqrt{\left(1+\frac{V_r}{V_o}\right)}}$$

2.6.3 DIFFUSION CAPACITANCE

If diode is forward biased, the potential barrier at the junction is lowered and holes from the p side enter the n side. Similarly, electrons from the n side move into the p side. This process is called minority- carrier injection. After injection the excess electron & hole density falls off exponentially with distance.

With change in the applied forward voltage, the concentration of injected charge particles changes which is a capacitive effect & the capacitance of this kind is called diffusion capacitance C_D. It is called the diffusion or storage capacitance

$C_D = \tau g$

where, g is dynamic conductance of diode

$$g = \frac{I_f}{\eta V_T}$$

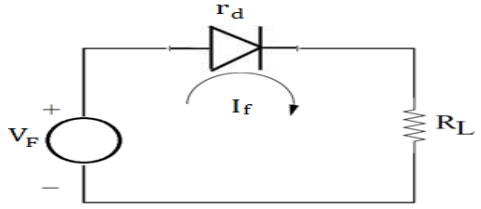
τ is minority carrier lifetime

$$\therefore C_D = \frac{\tau I_f}{\eta V_T}$$

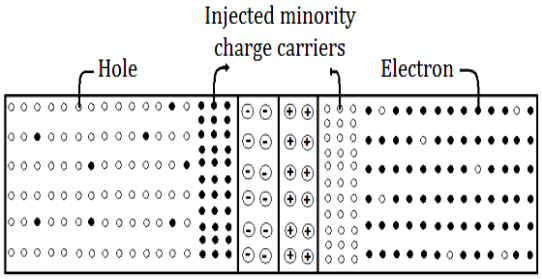
Note: Diffusion capacitance of diode increases exponentially with applied forward voltage.

2.7 DIODE SWITCHING

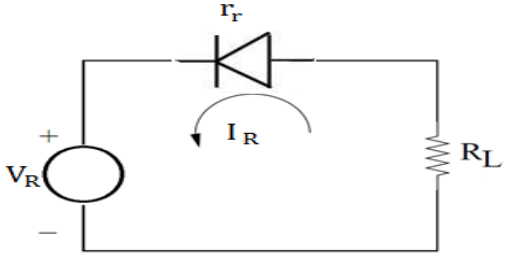
The transient response of a diode driven from an ON to an OFF state signifies that an interval of time elapses before the diode reaches its new steady state. Because it represents an important practical limitation, the reverse recovery i.e. switching from ON to OFF, is described below



In the forward- bias state large number of electrons from the n side injected into p side and large number of holes injected into n side from p side. Due to this diffusion process, large number of minority carriers will be there on either sides of the depletion layer. In a forward biased diode the forward resistance r_d is very small as compared to R_L hence the forward current through diode is $I_f \approx V_F / R_L$.The diode is operated in the same bias for a long time before $t = 0$.

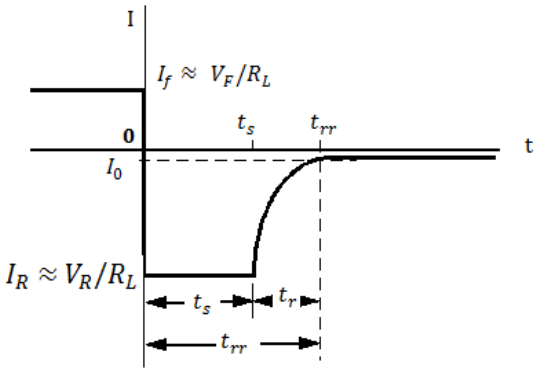


Now, if at $t = 0$ the polarity of the applied bias voltage is suddenly reversed to make the diode reverse biased then ideally the diode should change its condition from ON to OFF instantly.



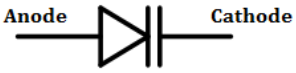
However for a practical diode, this does not happen because of large number of minority carriers on each sides of depletion layer in forward bias condition. When diode is suddenly reversed biased these injected charge carriers are swept back across the junction to the side from which they originated. This charge motion produces a current in the reverse direction. The period of time during which these minority carriers are swept back i.e. time between $t = 0$ and $t = t_s$, is called the **storage time** t_s. During this time interval the diode conducts (i.e. offers a very low resistance r_r unlike reversed biased diode) & a large reverse current $I_R \approx V_R / R_L$ flows through diode i.e diode remains in ON state.

After storage time $t=t_s$ (once all the injected minority carriers are swept back) the diode begins to reverse biased and the magnitude of the current decreases toward I_0 (i.e reverse saturation current). This time during which diode current decreases from I_R to I_0 is called **transition interval** denoted by t_r. The sum of storage time and transition interval is known as **reverse recovery time** t_{rr} for the diode.



The reverse recovery time depends on the RC time constant where C is a transition capacitance of a diode. Thus to have fast switching from ON to OFF of a diode, the transition capacitance should be as small as possible. Thus the transition capacitance plays an important role in the switching circuits using diodes.

2.8 VARACTOR DIODE

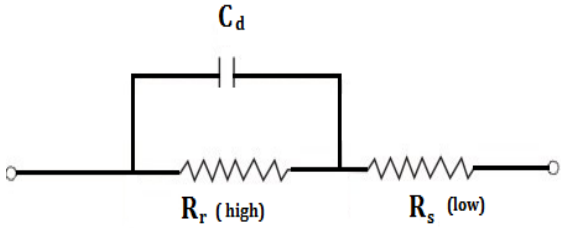


A varactor diode is a linearly graded diode & always operated in a reverse-biased state. No current flows, but since the thickness of the depletion zone varies with the applied bias voltage, the capacitance of the diode can be made to vary. Capacitance is inversely proportional to the depletion region thickness. Thus, the capacitance is inversely proportional to the root of applied voltage.

$$C_T \propto \frac{1}{\sqrt[3]{\text{R.B.voltage}}}$$

All diodes exhibit this phenomenon to some degree, but varactor diodes are manufactured specifically to exploit this effect and increase the capacitance (and thus the range of variability), whereas most ordinary diode fabrication strives to minimize the capacitance.

2.8.1 EQUIVALENT CIRCUIT



Where, C_d is depletion capacitance?

R_r is reverse resistance

R_s is contact resistance

2.8.2 APPLICATIONS

1) They are used in Parametric Amplifiers.
2) They are used for tuning receivers.
3) They are used as voltage controlled oscillators.

2.9 LIGHT EMITTING DIODE

A **light-emitting diode** (**LED**) is a two-lead semiconductor light source that resembles a basic pn-junction diode, except that an LED also emits light. LED is always fabricated with direct band gap semiconductor.

When an LED is forward biased, the majority charge carriers cross the junction & large no. of recombinations take place at the junction. Due to these recombination's energy is released in the form of light. This effect is called electroluminescence, and the color of the light (corresponding to the energy of the photon) is determined by the energy band gap of the semiconductor.

$$E_G = h\nu$$

$$E_G = \frac{hc}{\lambda}$$

$$\lambda = \frac{hc}{E_G}$$

$$\lambda = \frac{1.24}{E_G}\mu m$$

where, E_G is forbidden band gap of material (eV)

ν is frequency of emitted light

h is plank's constant

$h = 6.62\times10^{-34}\ m^2\ kg/s$

λ is wavelength in μm

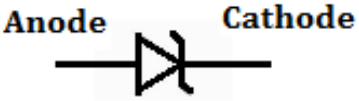
2.9.1 APPLICATIONS

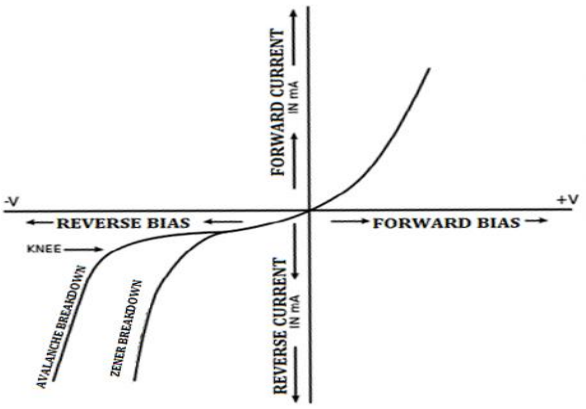
1) Visual signals where light goes more or less directly from the source to the human eye, to convey a message or meaning.
2) The light from LEDs can be modulated very quickly so they are used extensively in optical fiber and free space optics communications.
3) LEDs are also suitable for backlighting for LCD televisions.

2.10 ZENER DIODE

The Zener diode's operation depends on the heavy doping of its p-n junction allowing electrons to tunnel from the valence band of the p-type material to the conduction

band of the n-type material. In the atomic scale, this tunneling corresponds to the transport of valence band electrons into the empty conduction band states; as a result of the reduced barrier between these bands and high electric fields that are induced due to the relatively high levels of doping on both sides.





A Zener diode is a type of diode that permits current not only in the forward direction like a normal diode, but also in the reverse direction if the voltage is larger than the breakdown voltage known as Zener knee voltage or breakdown voltage. A Zener diode does not allow significant current if it is reverse-biased below its reverse breakdown voltage. When the reverse bias breakdown voltage is exceeded, a Zener diode is subject to high current due to breakdown. Unless this current is limited by circuitry, the diode will be permanently damaged.

In case of large forward bias (current in the direction of the arrow); the diode exhibits a voltage drop due to its junction built-in voltage and internal resistance. The amount of the voltage drop depends on the semiconductor material and the doping concentrations. A Zener diode exhibits almost the same properties, except the device is specially designed so as to have a greatly reduced breakdown voltage, the so-called Zener voltage. By contrast with the conventional device, a reverse-biased Zener diode will exhibit a controlled breakdown and allow the current to keep the voltage across the Zener diode at the Zener voltage. For example, a diode with a Zener breakdown voltage of 3.2 V will exhibit a voltage drop of 3.2 V even if reverse bias voltage applied across it is more than its Zener voltage.

2.10.1 ZENER BREAKDOWN

Zener breakdown occurs in heavily doped pn junctions. The heavy doping makes the depletion layer extremely thin. Due to thin depletion layer the electric field acting on depletion layer is very strong & due to this high electric field, there is direct rupture of covalent bonds & current through diode increases. Zener breakdown voltage is less than 7 volts.

The temperature coefficient of the Zener mechanism is negative i.e. the breakdown voltage for a particular diode decreases with increasing temperature.

2.10.2 AVALANCHE BREAKDOWN

Avalanche breakdown occurs in lightly doped diodes. It is caused by impact ionization of electron-hole pairs. In a reverse biased diode, electrons that enter the depletion region undergo a tremendous acceleration. As these accelerated carriers collide with the atoms they can knock electrons from their bonds, creating additional electron/hole pairs and thus additional current. As these secondary carriers are swept into the depletion region, they too are accelerated and the process repeats itself. This is akin to an avalanche where a small disturbance causes a whole mountainside of snow to come crashing down. Avalanche breakdown voltage is greater than 6 volts.

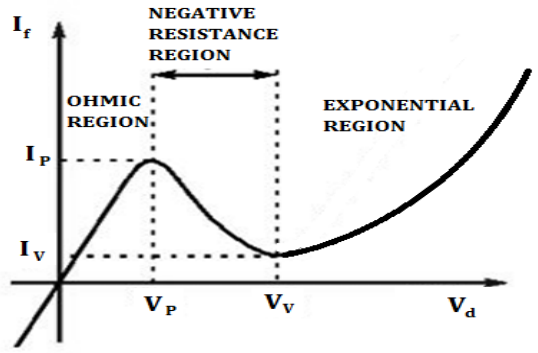
The temperature coefficient of the avalanche mechanism is positive i.e. the breakdown voltage for a particular diode increases with increasing temperature.

2.10.3 APPLICATIONS

1) The Zanier diode ideal for applications such as the generation of a reference voltage (e.g. for an amplifier stage).
2) They are used as a voltage stabilizer for low-current applications.

2.11 TUNNEL DIODE

In the tunnel diode, the semiconductor materials used in forming a junction are doped to the extent of one impurity atom per thousand atoms of semiconductor. This heavy doping produces an extremely narrow depletion zone similar to that in the Zener diode. Also because of the heavy doping, a tunnel diode exhibits an unusual current-voltage characteristic curve as compared with that of an ordinary junction diode. The characteristic curve for a tunnel diode is illustrated in figure below

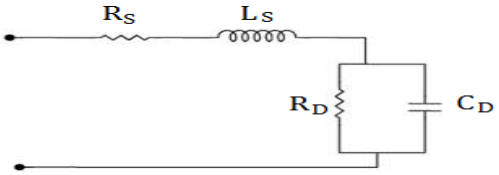


The three most important aspects of this characteristic curve are:

1) When $V_d < V_p$, the forward current increases linearly to a peak (I_p).
2) When $V_p \le V_d \le V_v$, with increase in forward voltage current decreases from I_p to I_v i.e. it exhibits negative resistance in this region.
3) When $V_d > V_v$, the normal increasing forward current with further increases in the bias voltage.

The portions of characteristics curve between I_p and I_v is the region of negative resistance. The negative resistance region is the most important and most widely used characteristic of the tunnel diode.

2.11.1 EQUIVALENT CIRCUIT



2.11.2 APPLICATIONS

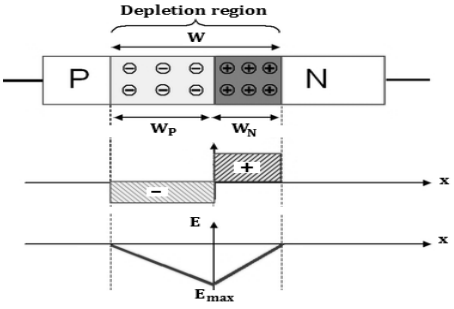
1) A tunnel diode biased to operate in the negative resistance region can be used as either an oscillator or an amplifier in a wide range of frequencies and applications.
2) Tunnel diodes are also used extensively in high-speed switching circuits because of the speed of the tunneling action.

2.12 TYPES OF PN JUNCTIONS

Based on the fabrication process there are several different types of PN junctions. Some of these are discussed below.

2.12.1 STEP GRADED PN JUNCTION

A step graded junction is also called as abrupt junction. In a step graded PN junction both the layers are uniformly doped but there is abrupt change in doping at the junction i.e. in a step graded junction P & N sides have different doping. A highly doped region is represented with a '+' superscript i.e. step graded junction is either P^+N or PN^+. The charge density & electric fields are shown in the figure below



As the depletion layer width is inversely proportional to doping concentration, it penetrates more into lightly doped region as compared to highly doped region. The depletion region width W_N, W_P & doping concentrations N_D, N_A on P & N sides are related by the charge neutrality equation as

$$\frac{W_N}{W_P} = \frac{N_A}{N_D}$$

Or $W_N N_D = W_P N_A$

The electric field across the depletion layer directs from N-side to P-side, it is maximum at the junction & it decreases as we move away from the junction. The magnitude of maximum electric field is given by

$$E_{max} = \frac{qN_D W_N}{\varepsilon} = \frac{qN_A W_P}{\varepsilon}$$

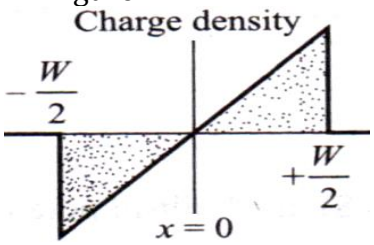
Where $\varepsilon = \varepsilon_0 \varepsilon_r$

$\varepsilon_0 = 8.854 \times 10^{-12} F/m$

ε_r is relative permittivity

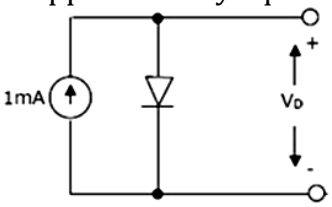
2.12.2 LINEARLY GRADED JUNCTION

In a linearly graded PN junction, the doping concentration does not abruptly change but the change is almost linearly across the junction. The width of depletion layer is same on both the sides. The depletion layer width varies as $V^{\frac{1}{2}}$ instead of $V^{\frac{1}{3}}$ as in the case of step graded junction. The charge density variation in linearly graded diode is as shown in figure.



GATE QUESTIONS

Q.1 In the figure, a silicon diode is carrying a constant current of 1 mA. When the temperature of the diode is 20°C, V_D is found to be 700 mV. If the temperature rises to 40°C, V_D becomes approximately equal to



a)740 mV b)660 mV
c)680 mV d)700 mV

[GATE-2002]

Q.2 Choose proper substitutes for X and Y to make the following statement correct. Tunnel diode and Avalanche photodiode are operated in X bias and Y bias respectively.
a) X: reverse, Y:reverse
b) X:reverse, Y:forward
c) X: forward , Y : reverse
d) X : forward , Y : forward

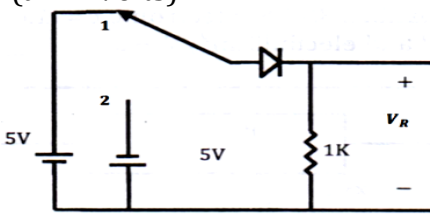
[GATE-2003]

Q.3 The values of voltage (V_D) across a tunnel–diode corresponding to peak and valley currents are V_p and V_V respectively. The range of tunnel-diode voltage (V_D) for which the slop of its I-(V_D) characteristics is negative would be

a) $V_D < 0$ b) $0 \le V_D < V_p$
c) $V_p \le V_D < V_V$ d) $V_D \ge V_V$

[GATE-2006]

Q.4 In the circuit shown below, the switch was connected to position 1 at t<0 and at t=0, it is changed to position 2. Assume that y the diode has zero voltage drop and a storage time t_s.For $0 < t \le t_s$ V_R is given by (all in Volts)



a) $V_R = -5$ b) $V_R = +5$
c)$0 \le V_R < 5$ d) $-5 < V_R < 0$

[GATE-2006]

Q.5 Find the correct match between Group 1 and Group 2

Group 1
E. Varactor diode
F. PIN diode
G. Zener diode
H. Scotty diode

Group 2
1. Voltage reference
2. High-frequency
3. Tuned circuits
4. Current controlled attenuator

a) E-4, F-2, G-1, H-3
b) E-2, F-4, G-1, H-3
c) E-3, F-4, G-1, H-2
d) E-1, F-3, G-2, H-4

[GATE-2006]

Q.6 In a p^+n junction diode under reverse bias, the magnitude of electric field is maximum at
a) the edge of the depletion region on the p-side
b) the edge of the depletion region on the n-side
c) the p^+n junction
d) the centre of the depletion region on the n-side

[GATE-2007]

Q.7 Group I lists four type of p-n junction diodes . Match each device in Group I with one of the Options in

Group II to indicate the bias condition of that device in its normal mode of operation

Group I	Group II
P. Zener diode	1)Forward Bias
Q. Solar cell	2) Reverse Bias
R. LASER Diode	
S. Avalanche Photodiode	

a)P-1,Q-2,R-1,S-2
b) P-2,Q-1,R-1,S-2
c) P-2,Q-2,R-2,S-1
d) P-2,Q-1,R-2,S-2

[GATE-2007]

Q.8 Group I lists four different semiconductor device. Match each device in Group I with characteristic property in Group II

Group I	Group II
P. BJT	1.Population inversion
Q. MOS Capacitor	2. Pinch off Voltage
R. Laser Capacitor	3. Early effect
S. JFET	4.Flat –band voltage

a)P-3, Q-1, R-4, S-2
b) P-1, Q-4, R-3, S-2
c) P-3, Q-4, R-1, S-2
d) P-3, Q-2, R-1, S-4

[GATE-2007]

Q.9 Ap$^+$n junction has built–in potential of 0.8 V. The depletion layer width at a reverse bias of 1.2V is 2 μm. For a reverse bias of 7.2 V, the depletion layer width will be

a) 4 μm b) 4.9 μm
c) 8 μm d) 12 μm

[GATE-2007]

Q.10 Which of the following is Not associated with a p-n junction?
a) Junction Capacitance
b)Charge Storage Capacitance
c) Depletion Capacitance
d) Channel Length Modulation

[GATE-2008]

Q.11 Consider the following assertions:
S1: for Zanier effect to occur, a very abrupt junction is required
S2: For quantum tunneling to occur, a very narrow energy barrier is required.
Which of the following is correct?
a) Only S2 is true
b) S1 and S2 are both true but S2 is not a reason for S1
c) S1 and S2 are both true and S2 is a reason for S1
d) Both S1 and S2 are false

[GATE-2008]

Q.12 Compared to a p-n junction with $N_A = N_D = 10^{14}/cm^3$, which one of the following statements is TRUE for a p-n junction with $N_A = N_D = 10^{20}/cm^3$?
a) Reverse breakdown voltage is lower and depletion capacitance is lower
b) Reverse breakdown voltage is higher and depletion capacitance is lower
c) Reverse breakdown voltage is lower and depletion capacitance is higher
d) Reverse breakdown voltage is higher and depletion capacitance is higher

[GATE-2010]

Q13 A silicon PN junction is forward biased with a constant current at room temperature. When the temperature is increased by 10°C, the forward bias voltage across the PN junction
a) Increase by 60mV
b) decrease by 60mV
c) Increase by 25mV
d) decrease by 25 mV

[GATE-2011]

Q.14 In a forward biased p-n junction diode, the sequence of events that best describes the mechanism of current flow is

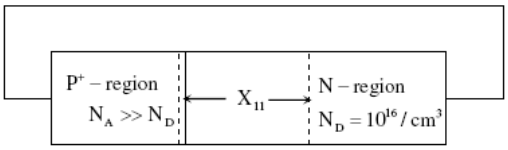
a) Injection, and subsequent diffusion and recombination of minority carriers
b) Injection, and subsequent drift and generation of minority carriers
c) Extraction, and subsequent diffusion and generation of minority carriers
d) Extraction, and subsequent drift and recombination of minority carriers

[GATE-2013]

Q.15 When the optical power incident on a photodiode is 10 μW and the responsivity is 0.8A / W, the photocurrent generated (in μA) is _____.

[GATE-2014-1]

Q.16 Consider an abrupt PN junction (at T = 300 K) shown in the figure. The depletion region width $X_{n.}$ on the N-side of the junction is 0.2 μm and the permittivity of silicon (ε_{si}) is 1.044×10^{-12} F/cm. At the junction, the approximate value of the peak electric field (in kV/cm) is _____.



[GATE-14-2]

Q.17 The donor and accepter impurities in an abrupt junction silicon diode are 1×10^{16} cm^{-3} and 5×10^{18} cm^{-3}, respectively. Assume that the intrinsic carrier concentration in silicon $n_i = 1.5 \times 10^{10}$ cm^{-3} at 300 K, $\frac{kT}{q} = 26$ mV and the permittivity of silicon $\varepsilon_{si} = 1.04 \times 10^{-12}$F/ cm. The built-in potential and the depletion width of the diode under thermal equilibrium conditions, respectively, are

a) 0.7 V and 1×10^{-4} cm
b) 0.86 V and 1×10^{-4} cm
c) 0.7 V and 3.3×10^{-5}cm
d) 0.86 V and 3.3×10^{-5}cm

[GATE-2014-3]

Q.18 A region of negative differential resistance is observed in the current voltage characteristics of a silicon PN junction if

a) Both the P-region and the N-region are heavily doped
b) The N-region is heavily doped compared to the P-region
c) The P-region is heavily doped compared to the N-region
d) An intrinsic silicon region is inserted between the P-region and the N-region

[GATE-2015]

Q.19 The built-in potential of an abrupt p-n junction is 0.75V. If its junction capacitance (C_J) at a reverse bias (V_R) of 1.25V is 5pF , the value of C_J (in pF) when V_R = 7.25V is _____.

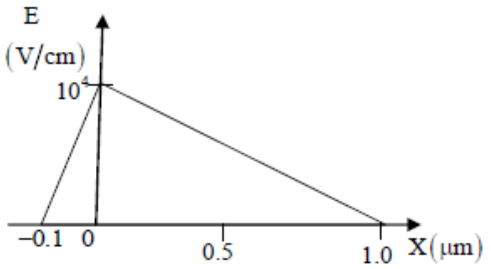
[GATE-2015]

Q.20 For a silicon diode with long P and N regions, the accepter and donor impurity concentrations are 1×10^{17} cm^{-3} and 1×10^{15} cm^{-3}, respectively. The lifetimes of electrons in P region and holes in N region are both 100μs . The electron and hole diffusion coefficients are 49 cm^2 / s and 36 cm^2 / s, respectively. Assume kT / q= 26 mV , the intrinsic carrier concentration is 1×10^{10} cm^{-3} and q $=1.6 \times 10^{-19}$ C . When a forward voltage of 208 mV is applied across the diode, the hole current density (in nA /cm^2) injected from P region to N regions is _____.

[GATE-2015-1]

Q.21 The electric field profile in the depletion region of a p-n junction in

equilibrium is shown in the figure. Which one of the following statements is NOT TRUE?



a) The left side of the junction is n-type and the right side is p-type
b) Both the n-type and p-type depletion regions are uniformly doped
c) The potential difference across the depletion region is 700 mV
d) If the p-type region has a doping concentration of 10^{15} cm^{-3} , then the doping concentration in the n-type region will be 10^{16} cm^{-3}

[GATE-2015-3]

Q.22 Consider a silicon p-n junction with a uniform acceptor doping concentration of $10^{17} cm^{-3}$ on the p-side and a uniform donor doping concentration of 10^{16} cm^{-3} on the n-side. No external voltage is applied to the diode. Given: kT/q = 26 mV, $n_i = 1.5 \times 10^{10}$ cm^{-3}, $\varepsilon_{si} = 12\varepsilon_0$, $\varepsilon_0 = 8.85 \times 10^{-14}$ F/m, and $q = 1.6 \times 10^{-19}$ C The charge per unit junction area (nC cm^{-2}) in the depletion region on the p-side is ___.

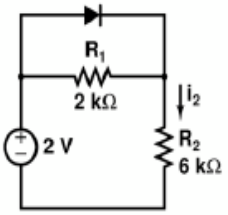
[GATE-2016-1]

Q.23 Consider avalanche breakdown in a silicon p^+ n junction. The n-region is uniformly doped with a donor density N_D. Assume that breakdown occurs when the magnitude of the electric field at any point in the device becomes equal to the critical field E_{crit} . Assume E_{crit} to be independent of N_D. .If the built-in voltage of the p+ n junction is much smaller than the breakdown voltage, V_{BR}, the relationship between V_{BR} and N_D is given by

a) $V_{BR} \times \sqrt{N_D}$ = constant
b) $N_D \times \sqrt{V_{BR}}$ = constant
c) $N_D \times V_{BR}$ = constant
d) N_D / V_{BR} = constant

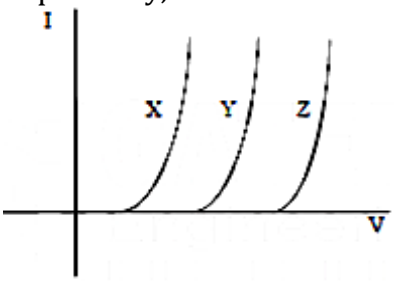
[GATE-2016-2]

Q.24 Assume that the diode in the figure has V_{on}= 0.7V, but is otherwise ideal. The magnitude of the current i_2 (in mA) is equal to _____.



[GATE-2016-2]

Q.25 The I-V characteristics of three types of diodes at the room temperature, made of semiconductors X, Y and Z, are shown in the figure. Assume that the diodes are uniformly doped and identical in all respects except their materials. If EgX, EgY and EgZ are the band gaps of X, Y and Z, respectively, then

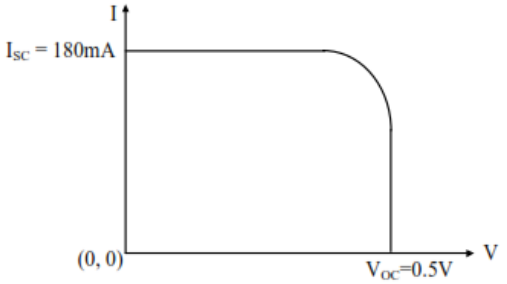


a) EgX > EgY > EgZ
b) EgX = EgY = EgZ
c) EgX < EgY < EgZ
d) no relationship among these band gaps exists

[GATE-2016-3]

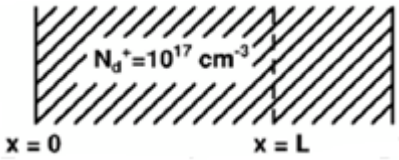
Q.26 The figure shows the I-V characteristics of a solar cell illuminated uniformly with solar light of power 100 mW/cm^2. The

solar cell has an area of 3 cm^2 and a fill factor of 0.7. The maximum efficiency (in %) of the device is ___.



[GATE-2016-3]

Q.27 Consider a region of silicon devoid of electrons and holes, with an ionized donor density of $N_d^+ = 10^{17}$ CM^{-3}. The electric field at x = 0 is 0 V/cm and the electric field at x = L is 50 kV/cm in the positive x direction. Assume that the electric field is zero in the y and z directions at all points.



Given q =1.6 × 10^{-19}coulomb, ϵ_0 = 8.85 × 10^{-14} F/cm, ϵ_r = 11.7 for silicon, the value of L in nm is ____.

[GATE-2016-2]

Q.28 The I-V characteristics of the zener diodes D1 and D2 are shown in Figure I. These diodes are used in the circuit given in Figure II. If the supply voltage is varied from 0 to 100 V, then breakdown occurs in

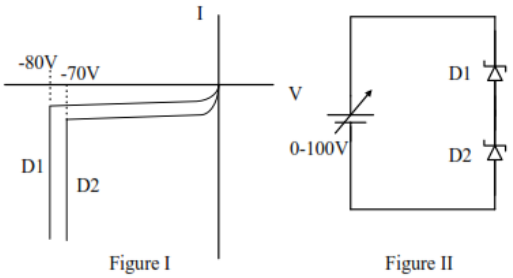


Figure I Figure II

a) D1 only b) D2 only
c) both D1and D2 d) none of D1 & D2

[GATE-2016-3]

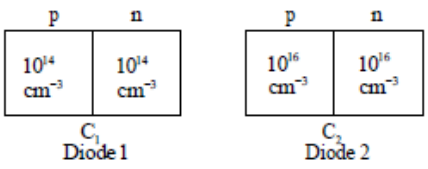
Q.29 An n^+ -n Silicon device is fabricated with uniform and non-degenerate donor doping concentrations of N_{D1} = 1 x $10^{18}cm^{-3}$ and N_{D2} = 1 x 10^{15} cm^{-3} corresponding to the and n^+ regions respectively. At the operational temperature T, assume complete impurity ionization, kT/q = 25 mV, and intrinsic carrier concentration to be n_1 = 1 x 10^{10} cm^{-3}. What is the magnitude of the built- in potential of this device?

a)0.748V b) 0.460V

c) 0.288V d) 0.173V

[GATE-2017-1]

Q.30 As shown, two Silicon (Si) abrupt p-n junction diodes are fabricated with uniform donor doping concentration of N_{D1} = $10^{14}cm^{-3}$ and N_{D2} = $10^{16}cm^{-3}$ in the n-regions of the diodes, and uniform acceptor doping concentration of N_{A1} = $10^{14}cm^{-3}$ and N_{A2} = $10^{16}cm^{-3}$ in the p-regions of the diodes, respectively. Assuming that the reverse bias voltage is >> built-in potentials of the diodes, the ratio C_2/C_1 of their reverse bias capacitances for the same applied reverse bias, is _____.



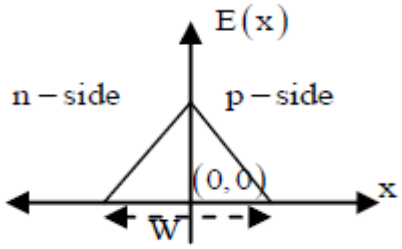
[GATE-2017-1]

Q.31 For a particular intensity of incident light on a silicon pn junction solar cell, the photocurrent density (JL) is 2.5 mA/cm2 and the open-circuit voltage (Voc) is 0.451 V. consider thermal voltage (VT) to be 25mV. If the intensity of the incident light is increased by 20 times, assuming that the temperature remains unchanged. Voc (in volts) will be _____.

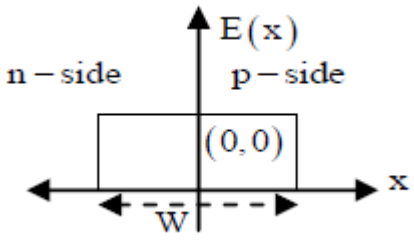
[GATE-2017-1]

Q.32 An abrupt pn junction (located at x = 0) is uniformly doped on both p and n sides. The width of the depletion region is W and the electric field variation in the x-direction is E(x). Which of the following figures represents the electric field profile near the pn junction?

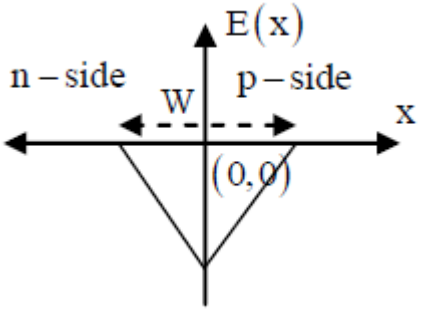
a)



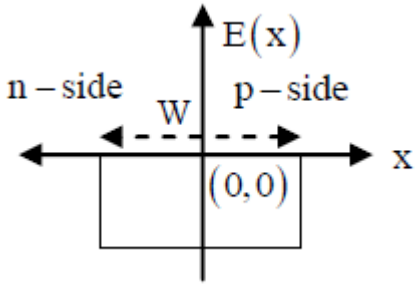
b)



c)



d)



[GATE-2017-2]

Q.33 A p-n step junction diode with a contact potential of 0.65 V has a depletion width 1μm of at equilibrium. The forward voltage (in volts, correct to two decimal places) at which this width reduces to 0.6 μm is___.

[GATE-2017-2]

Q.34 In a p-n junction diode at equilibrium, which one of the following statements is NOT TRUE?

a) The hole and electron diffusion current components are in the same direction.

b) The hole and electron drift current components are in the same direction.

c) ON an average, holes and electrons drift in opposite direction.

d) ON an average, electrons drift and diffuse in the same direction.

ANSWER KEY:

1	2	3	4	5	6	7	8	9	10	11	12	13	14
(b)	(c)	(c)	(a)	(c)	(c)	(b)	(c)	(a)	(d)	(a)	(c)	(d)	(a)
15	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**	**26**	**27**	**28**
8	30.6	(d)	(a)	2.5	28.6	(c)	*	(c)	0.25	(c)	21	32.4	(a)
29	**30**	**31**	**32**	**33**	**34**								
(d)	10	0.5262	(a)	0.416	(d)								

EXPLANATIONS

Q.1 **(b)**

For either Si or Ge $\frac{dV}{dT}$; $-2.5mV/℃$

In order to maintain a constant of I

$T_2 - T_1 = 40 - 20 = 20°C$

-2.5× 20mV=50mV

Therefore,

$V_D = 700 - 5$

=650≃660mV

Q.2 **(c)**

A tunnel diode is always operated under forward bias in negative resistance region & avalanche photo diode is operated in reverse bias.

Q.3 **(c)**

Varactor diodes are used in tuned circuits and zener diodes is used as voltage reference when it is in reverse bias. Scottky diode is used as high frequency switch.

Q.4 **(a)**

During storage time, diode will be ON so

V_R =-5V during $0 < t \leq t_s$.

Q.5 **(c)**

Between V_p and V_v voltage, tunnel diode acts as negative resistance.

Q.6 **(c)**

Electric field is max at the junction.

Q.7 **(b)**

Zener diode and avalanche photo diode –Reverse bias,

Solar cell and laser diode –forward bias.

Q.8 **(c)**

By the basic properties of various devices.

Q.9 **(a)**

Depletion width $w_{dep} \propto \sqrt{(V_o + V_R)}$

$w_{dep} = \sqrt{\frac{7.2+0.8}{1.2+0.8}} \times 2\mu$

$= 2 \times 2\mu$

$= 4\mu m$

Q.10 **(d)**

Channel length modulation is phenomena in MOSFET.

Q.11 **(a)**

Q.12 **(c)**

Zener breakdown voltage is lower for higher doping Depletion capacitance is inversely proportional to width of depletion and higher the doping lower width. So when doping is higher depletion capacitance is higher

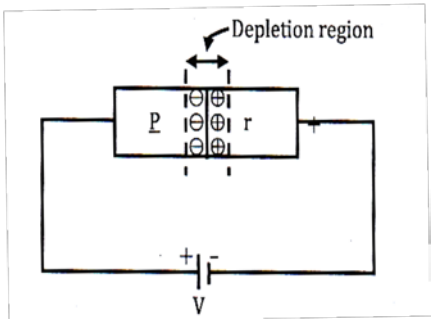
Q.13 **(d)**

For Si forward bias voltage by $-2.5mv/°C$

$10°C$ increase, change will be $-2.5 \times 10 = -25mV$

∴decrease by 25 mV

Q.14 **(a)**



In a forward biased p-n junction diode, the outward voltage force is applied , at first the minority carriers are injected through the depletion region that diffused

through the depletion region. As the minority carriers diffuse through the depletion region, they will recombine each other

Q.15 (8)

Responsivity (R) $=\frac{I_P}{P_0}$

$$0.8=\frac{I_P}{10\times10^{-6}}$$

$$\Rightarrow I_8=8\mu A$$

Q.16 (30.66)

Given $x_n = 0.2\mu m$, ϵ_{si} $= 1.044\times10^{-12}$ F / μ_n, $N_D = 10^{16}$ /cm^3

Peak Electric field, $E = \frac{qN_DX_n}{\epsilon}$

$$=\frac{1.6x10^{-19}\times10^{16}\times0.00002}{1.044\times10^{-12}}$$

$= 30.66$KV/cm

Q.17 (d)

$$V_{bi} = V_T \text{ In } \frac{N_AN_D}{n_i^2}$$

$$= 26 \text{ mv In } \left[\frac{5\times10^{18}\times1\times10^{16}}{\left(1.5\times10^{10}\right)^2}\right]$$

$= 0.859$V

$$W=\sqrt{\frac{2\varepsilon_s V_{bi}}{q}\left[\frac{N_A+N_D}{N_AN_D}\right]}$$

$$=3.34\times10^{-5}\text{cm}$$

Q.18 (a)

Q.19 (2.5)

$$C_J \propto \frac{1}{\sqrt{V_{bi}+V_R}}$$

$$\frac{C_{2J}}{C_{1j}}=\sqrt{\frac{V_{bi}+V_{R1}}{V_{bi}+V_{R2}}}$$

$$C_{2J}=C_{1j}\sqrt{\frac{2}{8}}=\frac{C_{1j}}{2}2.5\text{pF}$$

So, answer is 2.5

Q.20 (28.59)

Hole current density =

$$\frac{qD_pP_{n_0}}{L_p}\left(e^{\frac{qV_a}{kT}}-1\right)$$

$$P_{n_0}=\frac{n_i^2}{N_d}$$

Given $N_d = 1\times10^5\text{cm}^{-3}$

$\tau_p = \tau_n = 100\mu$ sec

$V_a = 208\text{mV}, D_p = 36, D_n = 49$

$$J_p=\frac{qn_i^2}{N_d}\sqrt{\frac{D_p}{\tau_p}}\left[e^{\frac{qV_a}{kT}}-1\right]$$

$$=\frac{1.6\times10^{-19}\times10^{20}}{1\times10^{15}}\sqrt{\frac{36}{100\mu}}\left[e^{\frac{208}{26}}-1\right]$$

$$=\frac{6\times10^2\times1.6\times10}{10^{15}}\times2.979\times10^3$$

$= 28.59$ nA/ cm^2

Q.21 (c)

Built in potential

$$\psi_0=\frac{1}{2}\times\left(10^6\,\text{V}/\text{m}\right)\times(1.1\times10^{-6}\text{m})$$

$=0.55$ volts

But in Question (option C) is given as 700 mV

Q.22 (47 to 49)

Q.23 (c)

If the depletion region is not making any change it means $N_D \times V_{BR}$ = constant

Q.24 (0.25)

Diode is the OFF state

$$I_2=\frac{2}{8k}=0.25\text{mA}$$

Q.25 (C)

Q.26 (21)

Efficiency = $\frac{FF.V_\infty I_{SC}}{P_{in}}$

$$=\frac{0.7\times0.5\times180}{(100\times3)}=21\%$$

Q.27 (32.37)

$$\frac{dE}{dx}=\frac{qN_D}{\in}\Rightarrow\frac{50\times10^3}{L}$$

$$=\frac{1.6\times10^{-19}\times10^{17}}{8.854\times10^{-14}\times11.7}$$

$$L=\frac{50\times10^3\times8.854\times10^{-14}\times11.7}{1.6\times10^{-2}}$$

$$=32.372\times10^{-9}\text{m}$$

Q.28 (a)

Q.29 (d)

$$V_{bi}=V_T\ln\left(\frac{N_1}{N_2}\right)$$

$$=0.25\ln\left(\frac{10^{18}}{10^{15}}\right)=0.173\text{V}$$

Q.30 10

$$C=\frac{\varepsilon A}{W}$$

$$C\propto\frac{1}{W}\text{and}W\propto\frac{1}{\sqrt{\text{doping}}}$$

$$C\propto\sqrt{\text{doping}}$$

$$\frac{C_2}{C_1}=\sqrt{\frac{(\text{doping})_1}{(\text{doping})_2}}=\sqrt{\frac{10^{16}}{10^{14}}}=\sqrt{100}=10$$

Q.31 0.51-0.54

$$J_s=\frac{J_L}{\left[e^{\frac{V_{OC}}{V_T}}-1\right]}$$

$$=\frac{2.5\text{x}10^{-3}}{\left[e^{\left(\frac{0.451}{0.025}\right)}-1\right]}$$

$$=3.6\text{x}10^{-11}\text{A}/\text{cm}^2$$

Now if the intensity of the light is increased by 20 times it means their photo current will also increase by 20 times

$$V_{OC}=\frac{kT}{q}\ln\left(\frac{J_L}{J_S}+1\right)$$

$$25\text{x}10^{-3}\ln\left(\frac{20\text{x}2.5\text{x}10^{-3}}{3.6\text{x}10^{-11}}+1\right)$$

$$=0.5262\text{Volt}$$

Q.32 (a)

If left side is p-region and right side is n-region then electric field triangle will be down warded and if the left side is n-region and right side is p-region, then electric field triangle will be upward.

Q.33 0.416

We know that in pn junction

$$W\propto\sqrt{V_{bi}-V_f}$$

Given,

$$W_1=1\mu\text{m},V_f=0$$

$$W_2=0.6\mu\text{m},V_f=?$$

$$\frac{W_1}{W_2}=\frac{5}{3}=\sqrt{\frac{0.65}{0.65-x}}$$

$$\frac{25}{9}\text{x}0.65\Rightarrow\frac{25}{9}\text{x}=0.65$$

$$x=0.416$$

Q.34 (d)

Since the concentration of holes on the p side is much greater than that in the n side, a very large hole diffusion current tends to flow across the junction from the p to the n material. Hence an electric field must build up across the junction in such a direction that a hole drift current will tend to flow across the junction from n to p side in order to

counterbalance the diffusion current.

3 TRANSISTORS

3.1 INTRODUCTION

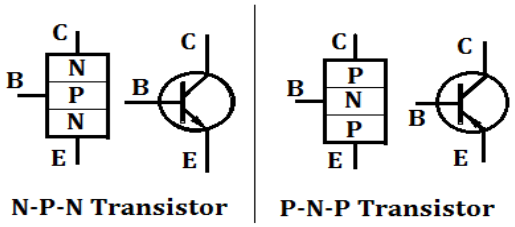
Transistors are active components and are found everywhere in electronic circuits. They are used as amplifiers and switching devices. As amplifiers, they are used in high and low frequency stages, oscillators, modulators, detectors and in any circuit needing to perform a function. In digital circuits they are used as switches. There are two types of junction transistors

1) Bipolar junction transistors: Bipolar transistors are so named because their operation involves both electrons and holes. These two kinds of charge carriers are characteristic of the two kinds of doped semiconductor material.

2) Unipolar junction transistors: Unipolar are called so because transistors such as the field-effect transistors have only one kind of charge carrier.

3.2 BIPOLAR JUNCTION TRANSISTOR

A bipolar junction transistor consists of a silicon (or germanium) crystal in which a layer of n-type silicon is sandwiched between two layers of p-type silicon. Alternatively a transistor may consist of a layer of p-type between two layers of n-type material. In the former case the transistor is referred to as a **p-n-p** transistor, and in the latter case, as an **n-p-n** transistor.

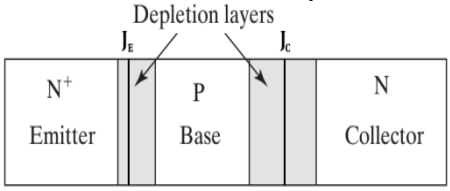


The three portions of a transistor are known as emitter, base and collector. The arrow on the emitter lead specifies the direction of current flow when the emitter –base junction is biased in the forward direction.

Emitter: Emits minority carriers into the base region of a BJT. For example, in an NPN BJT the n-type emitter emits electrons into the p-type base (electrons are called as minority charge carriers in P-type base). The emitter usually has the highest doping levels of the three regions in order to inject large number of minority charge carriers into base.

Base: Thin region which is used to control the flow of minority carriers from the emitter to the collector. Base is lightly doped in order to reduce the recombinations of injected minority carriers with the majority carriers of base region. Also base is smallest region in transistor so that a high concentration gradient for injected charge carriers can be created between base and collector.

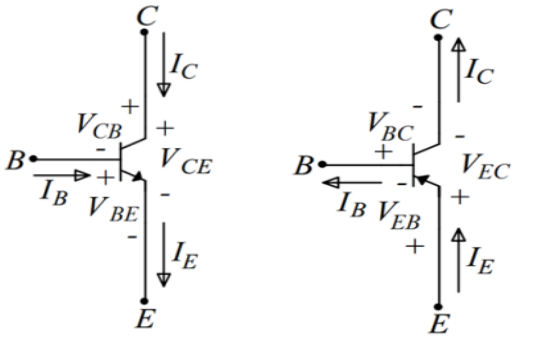
Collector: Collects the minority carriers that make it through the base from the emitter. The collector usually has moderate doping. It is the largest region of transistor in order to dissipate the heat generated at the reverse biased collector junction.



In BJT there are two junctions

1) J_E is called base emitter junction or simply emitter junction.
2) J_C is called base collector junction or simply collector junction.

As base is lightly doped region, the depletion region penetrates more into base region.



N-P-N Transistor P-N-P Transistor

In both cases the emitter, base and collector currents are I_E, I_B and I_C respectively. These are assumed positive when the current flows in the given direction.

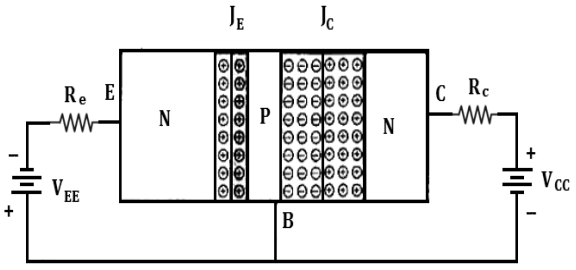
Also, $I_E = I_B + I_C$

The symbols V_{BE}, V_{CB} and V_{CE} are the emitter–base, collector-base, and collector–emitter voltages respectively. (More specifically, V_{BE} represents the voltage drop from base to emitter).

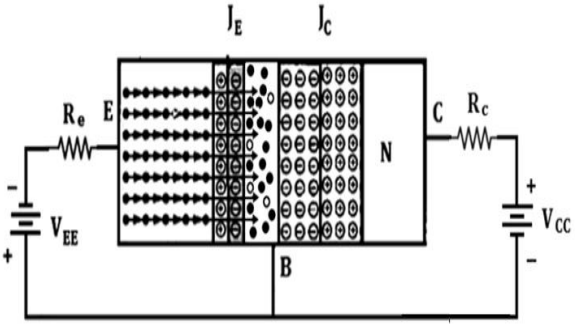
Also, $V_{CE} = V_{BE} + V_{CB}$

3.3 TRANSISTOR ACTION

Let us consider the n-p-n transistor for our discussion. The base to emitter junction is forward biased by the dc sourceV_{EE}. Thus, the depletion region at this junction is reduced. The collector to base junction is reverse biased, increasing depletion region at collector to base junction as shown Fig.



The forward biased BE junction cause the electrons in the n-type emitter to flow towards the base. This constitutes the emitter currentI_E. As these electrons flow through the p-type base, they tend to combine with holes in p-region (base). As the base is very thin and lightly doped, very few of the injected electrons recombine with holes to constitute base current(I_B).



The remaining large numbers .of electrons cross the depletion region and move through the collector region to the positive terminal of the external dc source. This constitutes collector currentI_C. Thus the electron flow constitutes the dominant current in an n-p-n transistor. Since the most of the electrons from emitter flow in the collector circuit and very few combine with hole in the base, the collector current is larger than the base current. Hence

$I_E = I_B + I_C$

3.4 TRANSISTOR CURRENT COMPONENTS

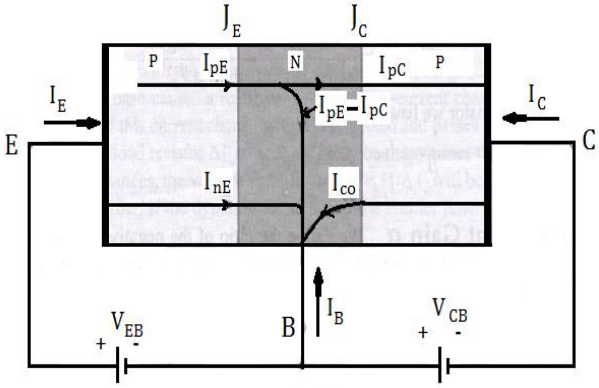


Fig. shows an n-p-n transistor with forward-biased emitter junction and the reverse –biased collector junction.

The emitter current I_E consists of hole current

1) I_{pE}: Due to holes crossing junction from emitter to base.
2) I_{nE}: Due to electrons crossing junction from base to the emitter.

In transistor the doping of the emitter is made much larger than the doping of the base. This feature ensures (in a p-n-p transistor) that the emitter current consists almost entirely of holes. Such a situation is desired since the current which results from electrons crossing the emitter junction from base to emitter does not contribute which can reach the collector.

Not all the holes crossing the emitter junction J_E reach the collector junction J_C because some of them combine with electrons in the n-type base. If I_{pC} is the hole current at J_C there must be a bulk recombination current $I_{pE}-I_{pC}$ leaving the base, as indicated in Fig (actually, electrons enter the base region through the base lead to supply those charges which have been lost by recombination with the holes injected into the base acrossJ_E).

If the emitter is open–circuited so that$I_E = 0$, then I_{pC} is also zero. Under these circumstances, the base and collector would act as a reverse–biased diode, and the collector current I_C would equal the reverse saturation currentI_{CO}.

i.e. if $I_E = 0$, then $I_C = I_{CO}$.

& if $I_E \neq 0$, then $I_C = I_{CO} - I_{pC}$

For a p-n-p transistor, I_{CO} consists of holes moving across J_C from left to right (base to collector) and electrons crossing J_C in the opposite direction. Since the assumed reference direction for I_{Co} in Fig is from right to left then for a p-n-p transistor I_{CO} is negative. For an n-p-n transistor, I_{CO} is positive.

3.4.1 EMITTER EFFICIENCY γ

The emitter, or injection, efficiency γ is defined as

$$\gamma = \frac{\text{current of injected carriersat } J_E}{\text{total emitter current}}$$

In the case of p-n-p transistor we

$$\gamma = \frac{I_{p^E}}{I_{p^E} + I_{n^E}} = \frac{I_{p^E}}{I_E}$$

In case of n-p-n transistor

$$\gamma = \frac{I_{nE}}{I_{p^E} + I_{n^E}} = \frac{I_{nE}}{I_E}$$

Where I_{pE} is the injected hole diffusion current at emitter junction and I_{nE} is the injected electron diffusion current at emitter junction.

3.4.2 TRANSPORTATION FACTOR β^*

The transport factor $\beta^*$is defined as

$$\beta^* \equiv \frac{\text{injected carrier current reaching } J_C}{\text{injected carriercurentat } J_E}$$

In the case of p-n-p transistor we have

$$\beta^* = \frac{I_{pC}}{I_{pE}}$$

In case of n-p-n transistor

$$\beta^* = \frac{I_{nC}}{I_{nE}}$$

3.4.3 LARGE SIGNAL CURRENT GAIN α

The ratio of the negative of the collector – current increment to the emitter-current change from zero (cutoff) to I_E as the large-signal current gain of a common-base transistor, or

$$\alpha = \frac{I_C - I_{Co}}{I_E}$$

Since I_C and I_E have opposite signs, then α as defined, is always positive. Typical numerical values of α lie in the range of 0.90 to 0.995.

$$\alpha = \frac{I_{pC}}{I_E} = \frac{I_{pC}}{I_{pE}} \frac{I_{pE}}{I_E}$$

$$\therefore \alpha = \beta^* \gamma$$

The transistor alpha is the product of the transport factor and the emitter efficiency. It should be pointed out that α is not a constant, but varies with emitter current I_E collector voltage V_{CB} and temperature.

If the transistor is in active region, the collector current is given by

$$I_C = \alpha I_E + I_{Co}$$

3.4.4 COLLECTOR REVERSE SATURATION CURRENT I_{CBO}

The collector current in a physical transistor when the emitter current is zero is designated by the symbol I_{CBO}. It increases approximately by 7% with one degree rise in temperature & it doubles for every 10^o rise in temperature.

Note: The actual collector current with collector junction reverse biased & base open-circuited is denoted as I_{CEO}.

Also, $I_{CEO} = (1+\beta) I_{CBO}$

3.5 EARLY EFFECT

An increase in magnitude of collector voltage increases the depletion width at the output junction diode & such action causes the effective base width W to decrease, this phenomenon known as the Early effect. This decrease in W has two consequences

1) There is less chance for recombination within the base region. Hence the transport factor β^* increases with an increase in the magnitude of the collector junction voltage.
2) Alsoα increases with an increase in the magnitude of the collector junction voltage.
3) The charge gradient is increases within the base, and consequently the current of minority carriers injected across the emitter junction increases i.e. I_C increases.

When the base–collector voltage reaches a certain (device specific) value, the base–collector depletion region boundary meets the base–emitter depletion region boundary. When in this state the transistor effectively has no base. The device thus loses all gain when in this state &this situation is called punch through or reaches through. When this situation occurs, a large collector current flows (breakdown) which may destroy transistor.

3.6 OPERATING REGIONS OF BJT

1) FORWARD ACTIVE

The base–emitter junction is forward biased and the base–collector junction is reverse biased. Most bipolar transistors are designed to afford the greatest common-emitter current gain, β_F, in forward-active mode. If this is the case, the collector–emitter current is approximately proportional to the base current, but many times larger, for small base current variations.

$I_C = \beta I_B + (1+\beta) I_{CBO}$

But, $I_{CBO} \ll 1$

$\therefore \quad I_C = \beta I_B$

Note:

For an N-P-N silicon transistor operating in active region $V_{BE} \geq 0.7$ V (for gemanium $V_{BE} \geq 0.2$ V)

2) SATURATION

With both junctions forward-biased, a BJT is in saturation mode and facilitates high current conduction from the emitter to the collector (or the other direction in the case of NPN, with negatively charged carriers flowing from emitter to collector). This mode corresponds to a logical "on", or a closed switch.

Note:

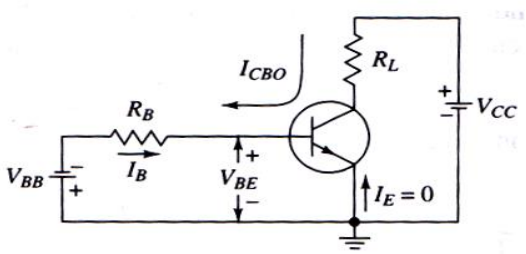
- In saturation region, collector current I_C is **no**t proportional to base current I_B. Hence $I_C = \beta I_B$ this equation is not valid in saturation.
- For an N-P-N silicon transistor operating in saturation $V_{BE} \geq 0.7$ V & $V_{CE} \leq 0.2$ V (for germanium $V_{BE} \geq 0.2$ V&$V_{CE} \leq 0.1$ V).

3) CUT-OFF

In cutoff, biasing conditions opposite of saturation (both junctions reverse biased) are present. There is very little current, which corresponds to a logical "off", or an open switch.

Note:

- In cut-off region $I_E = 0$& a small reverse current I_{CBO} flows through transistor as shown in figure



- For an N-P-N germanium transistor to operate in cutoff
  $V_{BE} = -V_{BB} + R_B I_{CBO} \leq -0.1V$
- For an N-P-N silicon transistor to operate in cutoff
  $V_{BE} = -V_{BB} + R_B I_{CBO} \leq 0.0V$

4) REVERSE ACTIVE

By reversing the biasing conditions of the forward-active region, a bipolar transistor goes into reverse-active mode. In this mode, the emitter and collector regions switch roles. Because most BJTs are designed to maximize current gain in forward-active mode, the β_F in inverted mode is several times smaller (2–3 times for the ordinary germanium transistor).

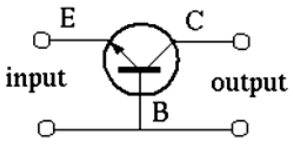
Typical values of junction voltages for N-P-N Transistor

	$V_{CE,sat}$	$V_{BE,sat}$	$V_{BE,active}$	$V_{BE,cutoff}$
Si	0.2	0.8	0.7	0.0
Ge	0.1	0.3	0.2	-0.1

3.7 OPERATING MODES OF BJT

Depending on which of the three terminals is used as common terminal, there can be three possible configurations for the two-port network formed by a transistor: common emitter (CE), common base (CB), and common collector (CC).

3.7.1 COMMON BASE CONFIGURATION



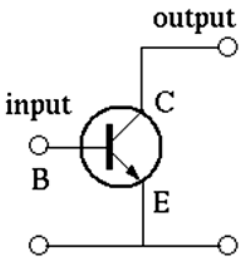
Here the input signal which is to be amplified is applied between emitter & base while output signal is taken between collector & base. The o/p current in this case is I_C& the i/p current is I_E.

Current gain of common base transistor is

$$\propto = \frac{I_C}{I_E}$$

$\propto \approx 1$, but it is always less than 1

3.7.2 COMMON EMITTER CONFIGURATION

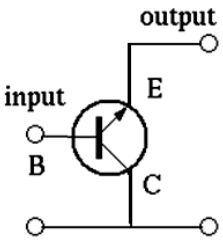


Here the input signal which is to be amplified is applied between base & emitter while output is taken between collector & emitter. The o/p current in this case is I_C& the i/p current is I_B.

Current gain of common emitter transistor is

$$\beta = \frac{I_C}{I_B}$$

3.7.3 COMMON COLLECTOR CONFIGURATION



Here the input signal which is to be amplified is applied between base & collector while output signal is taken between emitter & collector. The o/p

current in this case is I_E& the i/p current is I_B.

Current gain of common collector transistor is

$$\gamma = \frac{I_E}{I_B}$$

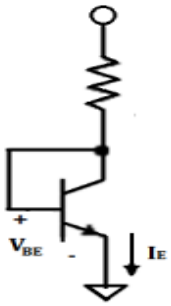
3.7.4 RELATION BETWEEN ∝, β&γ

1) $\propto = \frac{\beta}{1+\beta}$
2) $\beta = \frac{\propto}{1-\propto}$
3) $\gamma = 1+\beta$
4) $\gamma = \frac{1}{1-\propto}$

3.8 APPLICATIONS OF BJT

1) As a diode

BJT can be used as a diode by shorting the base & collector terminals. Another way to use BJT as diode is by keeping base & collector terminals at same potential. Due the short circuit across collector junction there will be only one PN junction (J_E).



When base & collector terminal are shorted, the emitter current through BJT is given by

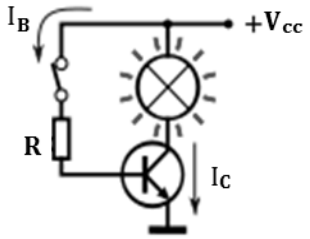
$$I_E = I_{CO} e^{V_{BE}/V_T}$$

Where, I_{CO} is reverse saturation current
$V_{BE}$is base to emitter voltage
$V_T$is thermal voltage

2) As a switch

Transistors are commonly used as electronic switches, both for high-power applications such as switched-mode power supplies and for low-power applications such as logic gates.

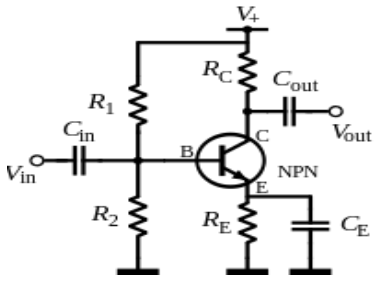
In a grounded-emitter transistor circuit, such as the light-switch circuit shown, as the base voltage rises, the emitter and collector currents rise exponentially. The collector voltage drops because of reduced resistance from collector to emitter. If the voltage difference between the collector and emitter were zero (or near zero), the collector current would be limited only by the load resistance (light bulb) and the supply voltage. This is called saturation because current is flowing from collector to emitter freely. When saturated, the switch is said to be **ON**& when it is in cut-off, the switch is said to be **OFF**.



3) As an amplifier

The common-emitter amplifier is designed so that a small change in voltage (V_{in}) changes the current through the base of the transistor & hence the current through collector. The transistor's current amplification combined with the properties of the circuit mean that small swings in V_{in} produce large changes in V_{out}.

Various configurations of single transistor amplifier are possible, with some providing current gain, some voltage gain, and some both.



3.9 FIELD EFFECT TRANSISTOR

The field-effect transistors a semiconductor device which depends for its operation on the control of current by an electric field.

There are two types of field-effect transistors, the junction field–effect transistor (abbreviated JFET, or simply FET) and the insulated–gate field–effect transistor (IGFET), more commonly called the metal-oxide-semiconductor (MOS) transistor(MOST or MOSFET).

3.9.1 ADVANTAGES OF FET OVER BJT

1) Its operation depends upon the flow of majority carriers only. It is therefore a unipolar (one type of carrier) device. The vacuum tube is another example of a unipolar device. The conventional transistor is a bipolar device.
2) It is relatively immune to radiation.
3) It exhibits a high input resistance, typically many mega-ohms.
4) It is less noisy than a tube or a bipolar transistor.
5) It exhibits no offset voltage at zero drain current, and hence makes an excellent signal chopper
6) It has excellent thermal stability.

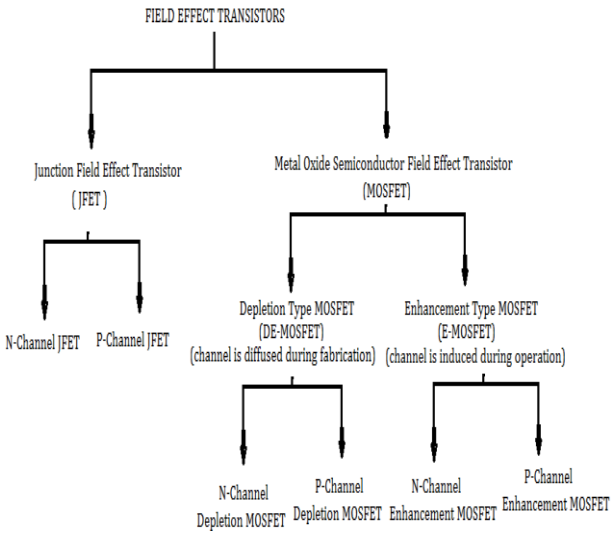
Note:

- BJT is a current controlled device while FET is a voltage controlled device.
- Unlike BJT, FET is a symmetrical device hence source & drain terminals can be interchanged.

3.9.2 DISADVANTAGE

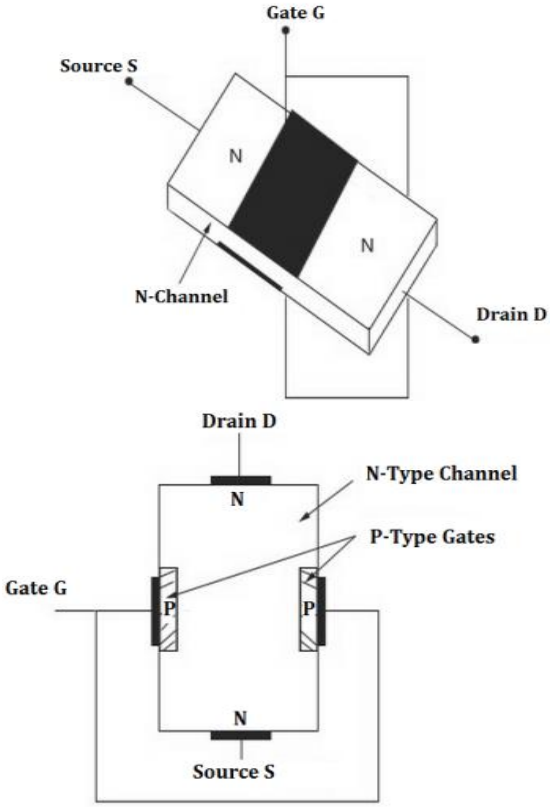
The main disadvantage of the FET is its relatively small gain–bandwidth product in comparison with that which can be obtained with a conventional transistor.

3.9.3 CLASSIFICATION OF FET's



3.10 JUNCTION FIELD EFFECT TRANSISTORS

The structure is quite simple. In an N-channel JFET an N-type silicon bar, referred to as the channel, has two smaller pieces of P-type silicon material diffused on the opposite sides of its middle part, forming P-N junctions, as illustrated in figure. The two P-N junctions forming diodes or gates are connected internally and a common terminal, called the gate terminal, is brought out.



The silicon bar behaves like a resistor between its two terminals D and S. The gate terminal is analogous to the base of an ordinary transistor (BJT). It is used to control the flow of current from source to drain. Thus, source and drain terminals are analogous to emitter and collector terminals respectively of a BJT.

In the figure above, the gate is P-region, while the source and the drain are N-regions. Because of this, a JFET is similar to two diodes. The gate and the source form one of the diodes, and the drain form the other diode. These two diodes are usually referred as the gate-source diode and the gate-drain diode. Since JFET is a silicon device, it takes only 0.7 volts for forward bias to get significant current in either diode. P-channel JFET is similar in construction to N-channel JFET except that P-type semiconductor material is sandwiched between two N-type semiconductors.

With the gate terminal not connected, and a potential applied (+ ve at the drain and – ve at the source), a current called the drain current, I_D flows through the channel located between the two P-regions. This current consists of only majority carriers-electrons in this case.

Source

The source S is the terminal through which the majority carriers enter the bar. Conventional current entering the bar at S is designated byI_S.

Drain

The drain D is terminal through which the majority carriers leave the bar. Conventional current entering the bar at D is designated by I_D.

Gate

On both sides of the n-type bar of fig. heavily doped (p^+) regions of acceptor impurities have been formed by alloying, by diffusion or by any other procedure available for creating p-n junctions. These impurity regions are called the gate G. Between the gate and source a voltage V_{GS} is applied in the direction to reverse-bias the p-n junction. Conventional current entering the bar at G is designatedI_G.

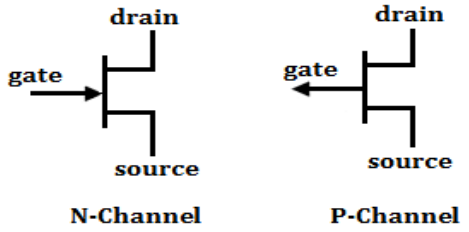
Note

As the junctions between gate-source & gate-drain are always kept reverse biased, the gate current entering the gate terminal in negligibly small & considered as 0

i.e. $I_G \approx 0$ A

Channel

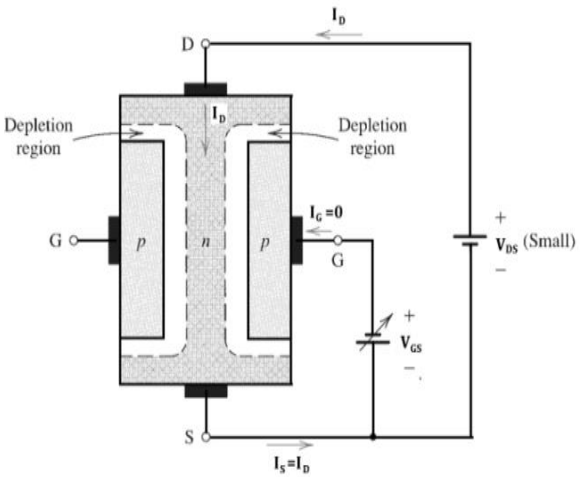
The region in fig of n-type material between the two gate regions is the channel through which the majority carriers move from source to drain.



3.10.1 OPERATION

Consider an N-channel JFET shown in figure.

When neither any bias is applied to the gate (i.e. when $V_{GS} = 0$) nor any voltage to the drain with respect to source (i.e. when $V_{DS} = 0$), the depletion regions around the P-N junctions, are of equal thickness and symmetrical.



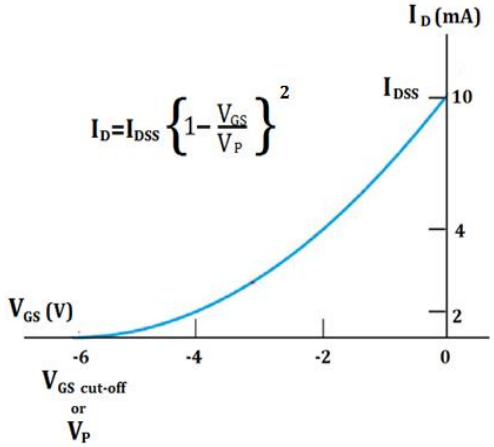
3.10.2 TRANSFER CHARACTERISTICS:

(Varying V_{GS} & keeping V_{DS} constant)

1) When $\mathbf{V_{GS} = 0\ V}$, the application of V_{DS} causes a current to flow from source to drain. The drain current in this case is maximum as the channel resistance is minimum & it is denoted as I_{DSS}.

2) When **negative V_{GS}** is applied, the depletion region of the gate-channel junction widens & the channel becomes correspondingly narrower; thus the channel resistance increases & the current I_D (for a given V_{DS}) decreases.
3) If we keep increasing V_{GS} in the negative direction, a value is reached at which the depletion region occupies the entire channel. At this value of V_{GS} the channel is completely depleted of charge carriers (electrons) & drain current reduces to zero. This value of V_{GS} is called cut-off voltage $V_{GS(cut-off)}$ or pinch-off voltage V_P.

Note: This variation in width of channel with applied V_{GS} is called channel width modulation.



The relationship between the drain current I_D and gate to source voltage V_{GS} is non-linear. This relationship is defined by Shockley's equations

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_p}\right)^2$$

In the equation values of I_{DSS} and V_p are constants, value of V_{GS} controls I_D

$I_D = 0$ when $V_{GS} = V_{GS(cut-off)}$

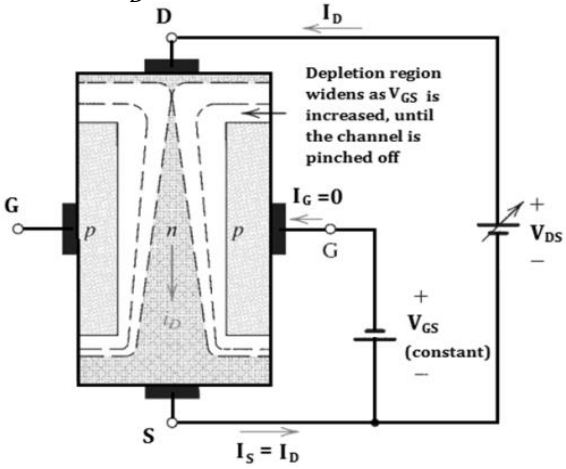
$I_D = I_{DSS}$ when $V_{GS} = 0$

Note: As the drain current depends on square of V_{GS}, a jfet can be called as a square law device.

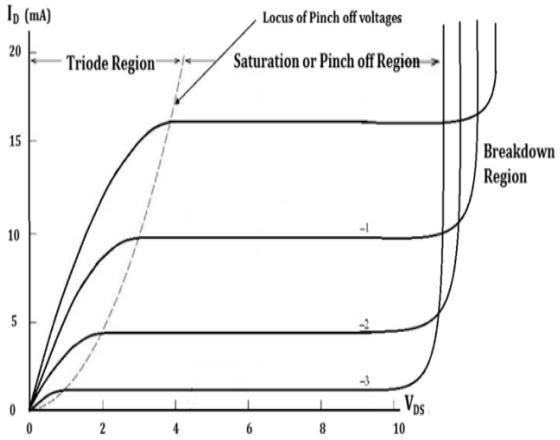
3.10.3 DRAIN CHARACTERISTICS

(Varying V_{DS} & keeping V_{GS} constant)

1) When $\boldsymbol{V_{DS} = 0\ V}$ the electric field in the channel is zero & the drain current I_D is zero.
2) When a positive voltage is applied to the drain terminal with respect to the source terminal i.e. $\boldsymbol{V_{DS} > 0\ V}$ is applied, a field is induced in the channel & electrons flow from source to drain results in drain current.
3) With increase in V_{DS} the reverse biasing of gate to drain increases and the depletion layer widens as shown in figure. Also the field in channel increases with V_{DS} & hence drain current I_D increases.



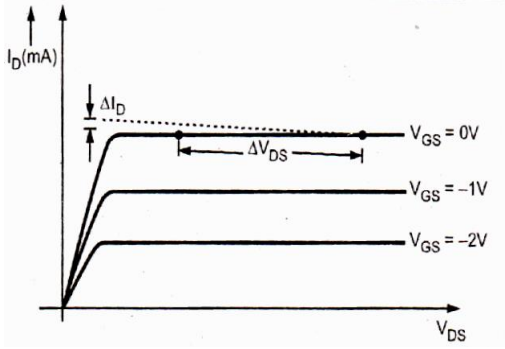
4) For a particular value of V_{DS} called pinch off voltage, both the depletion layers come extremely closer to each other but due to a very strong electric field the flow of charge carriers continue in the channel & drain current saturates.
5) For $V_{DS} > V_P$, the drain is almost constant



6) If V_{DS} is increased to a very large value above pinch off, jfet breaks down due to avalanche effect.

3.10.4 DRAIN RESISTANCE

From the drain characteristic, the important parameter of JFET, drain resistance $\boldsymbol{r_d}$,can be calculated fig. shows the drain characteristics of n-channel JFET



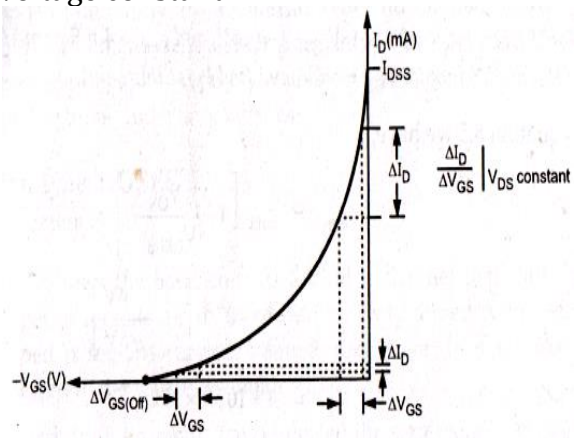
The drain resistance $\boldsymbol{r_d}$is the ac resistance between drain and source terminals when the JFET is operating in the saturation region. It is reciprocal of the slope of the drain characteristic in the saturation region. It is given by

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D}\Big|_{V_{GS}=\text{constant}}$$

Since the characteristics in the saturation region is almost flat, $\mathbf{r_d}$ is not easily determined from the characteristics. Value of $\mathbf{r_d}$ ranges from 50kΩ to several hundredkΩ. Since $\mathbf{r_d}$is usually the output resistance of the JFET.

3.10.5 TRANSCONDUCTANCE

The trans conductance, g_m, is the change in the drain current with change in gate to source voltage with the drain to source voltage constant.



From fig .we can say that it is the slope of the transfer characteristic. Since the slope varies g_m also varies. $g_m$has a greater value near the top of the curve than it does near the bottom. The transconductance g_m is defined as

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}\Big|_{V_{DS}\text{constant}}$$

The transconductance g_m is also called **mutual conductance.** The practical unit for g_m is mS or mA/V. For given g_m we can calculate an approximate value for g_m at any point on the transfer characteristic curve using the following equation .

$$g_m = g_{mo}\left[1 - \frac{V_{GS}}{V_{GS(off),}}\right]$$

Where g_{mo} is the value of g_m for $V_{GS} = 0$ and is given by,

$$g_{mo} = \frac{-2I_{DSS}}{V_P}$$

3.10.6 AMPLIFICATION FACTOR μ

Amplification factor $\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}\Big|_{I_D\text{constant}}$

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$$

$$= \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}}$$

$\therefore \quad \mu = r_d \times g_m$

Example

Data sheet of a JFET indicates that $I_{DSS} = 10mA$ and $V_{GS(cut-off),} = -4V$

Determine the drain current for $V_{GS} = 0V, -1V and -4V$.

Solution

For $V_{GS} = 0V, I_D = I_{DSS} = 10mA$

For $V_{GS} = -1,$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off),}}\right)^2$$

$$= 10mA\left(1 - \frac{-1}{-4}\right)^2$$

$$= 10 \times 10^{-3}[1 - 0.25]^2$$

$$= 10 \times 10^{-3} \times 0.5625$$

$$= 5.625mA$$

For $V_{GS} = -4V$

$$I_D = 10mA\left(1 - \frac{-4V}{-4V}\right)^2$$

$$= 10 \times 10^{-3}[1-1]^2 = 10 \times 10^{-3}(0)^2$$

$$= 0mA$$

Example

For JFET, if $I_{DSS} = 20mA, V_{GS(CUT-off),}$

$= -5V, and g_{mo} = 4mA/V.$

Determine the trans conductance for $V_{GS} = -4V$ and find I_D at the point.

Solution

we have ,

$$g_m = g_{mo}\left[1 - \frac{V_{GS}}{V_{GS(off),}}\right]$$

$$= 4 \times 10^{-3}\left[1 - \frac{-4V}{-5V}\right]$$

$$= 4 \times 10^{-3} \times 0.2$$

$$= 0.8mS$$

Also,

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off),}}\right]^2$$

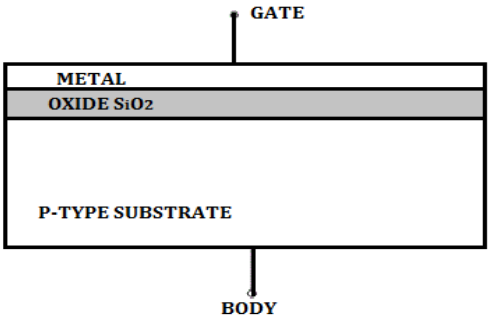
$$= 20 \times 10^{-3}\left[1 - \frac{-4V}{-5V}\right]^2$$

$$= 20 \times 10^{-3} \times 0.04$$

$$= 0.8mA$$

3.11 MOS CAPACITOR

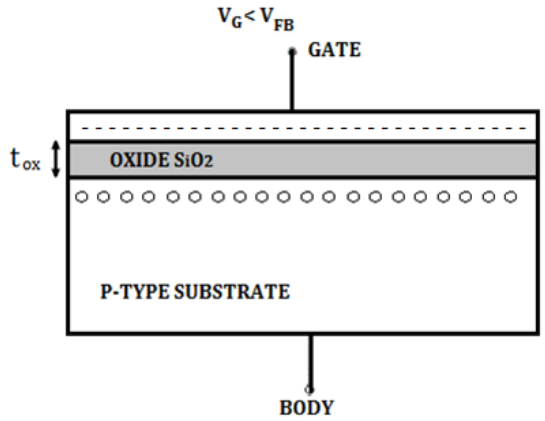
The MOS capacitor structure is shown in Figure 1. The "metal" plate is a heavily doped p^+ poly-silicon layer which behaves as a metal. The insulating layer is silicon dioxide and the other plate of the capacitor is the semiconductor layer which in our case is p-type silicon. The



The capacitance depends on the voltage that is applied to the gate (with respect to the body). Depending on the gate voltage the operation of MOS capacitor can be divided into three modes

3.11.1 ACCUMULATION MODE

When the applied gate voltage $V_G < V_{FB}$, (a negative voltage at gate) the majority charge carriers (holes) in the P-type substrate accumulates near the oxide semiconductor interface.



In accumulation mode, the capacitance in given by

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} F/m^2$$

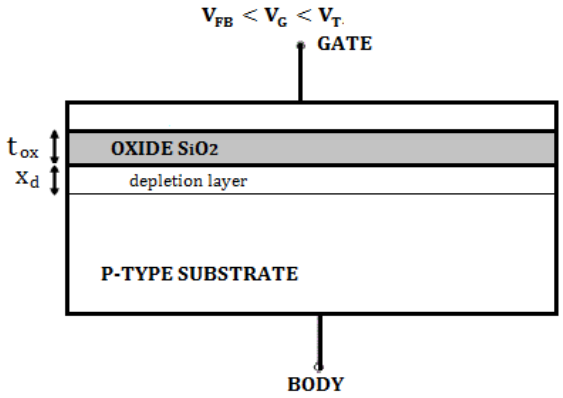
where, $\varepsilon_{ox} = 3.9\varepsilon_0$ is the permittivity of oxide layer

$\varepsilon_0 = 8.85 \times 10^{-12} F/m$

Note: With N-type substrate, there will be accumulation of electrons.

3.11.2 DEPLETION MODE

When $V_{FB} < V_G < V_T$ (small positive gate voltage), the positively charged carriers will be repelled away from the oxide semiconductor interface (note that this voltage is not sufficiently strong to attract the minority charge carriers in the substrate) & a depletion region is formed which is devoid of any mobile carriers leaving only ions.



In depletion mode there will be two capacitances in series

1) Oxide capacitance

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} F/m^2$$

2) Depletion capacitance

$$C_d = \frac{\varepsilon_{si}}{x_d} F/m^2$$

Where, $\varepsilon_{si} = \varepsilon_0\varepsilon_r$ is the permittivity of Silicon substrate

x_d is width of the depletion layer

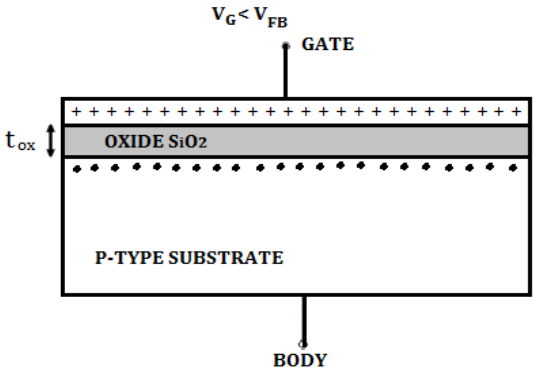
The total capacitance (F/m^2) in the depletion mode will be

$$C = \frac{C_{ox} \times C_d}{C_{ox} + C_d}$$

$$= \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_d}} = \frac{1}{\frac{t_{ox}}{\varepsilon_{ox}} + \frac{x_d}{\varepsilon_{si}}}$$

3.11.3 INVERSION MODE

When $V_G \geq V_T$, the minority charge carriers in the p-type substrate (electrons) are attracted towards oxide semiconductor interface i.e. an inversion layer of negatively charged carriers is formed.In inversion mobile carriers of the opposite type to the body aggregate at the surface to invert the conductivity type.



Note: With N-type substrate, inversion layer is formed due to holes.

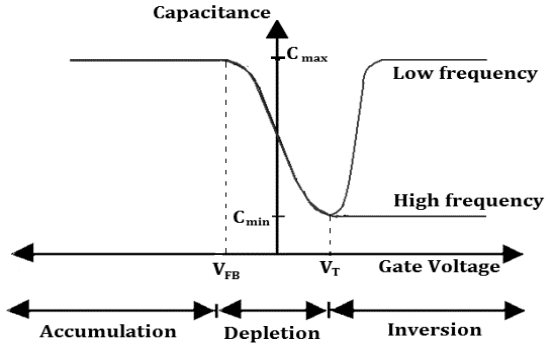
In inversion mode, the capacitance in given by

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} F/m^2$$

The two voltages that separate the three modes are

a) Flat band Voltage V_{FB} which separates the accumulation mode from the depletion mode
b) Threshold Voltage V_T which separates the depletion mode from the inversion mode.

3.11.4 CAPACITANCE CURVE



Where, $C_{max} = C_{ox}$

$$C_{min} = \frac{C_{ox} \times C_{dmin}}{C_{ox} + C_{dmin}}$$

C_d will be minimum when x_d is maximum.

Note: At high frequency (of gate voltage), inversion layer cannot form hence for high frequency the capacitance remain minimum in inversion mode also.

Example

The oxide thickness is 100 nm. Assume MOS has area of 1 cm². Calculate C_{ox}.

Solution

we know,

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} F/m^2$$

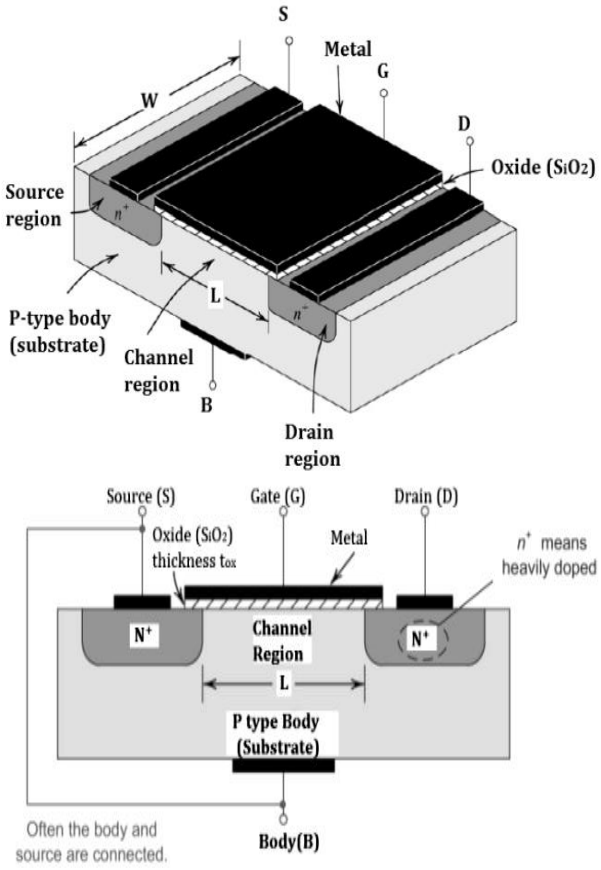
$$C_{ox} = \frac{\varepsilon_{ox} \times A}{t_{ox}} F$$

$$\varepsilon_{ox} = 3.9\varepsilon_0$$

$$\therefore C_{ox} = \frac{3.9 \times 8.85 \times 10^{-14} (F/cm) \times 1cm^2}{10^{-5} cm}$$

$$= 3.47 \times 10^{-8} F$$

3.12 METAL OXIDE SEMICONDUCTOR FET

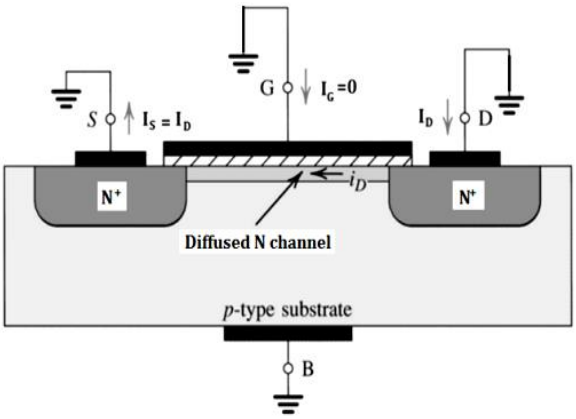


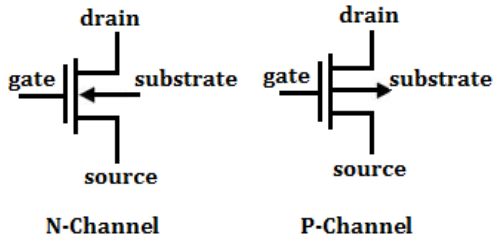
MOSFET stands for metal oxide semiconductor field effect transistor. It has four terminals gate, source drain and substrate or body. The drain and source terminals are connected to the heavily doped regions. The gate terminal is connected top on the oxide layer. The oxide layer results in an extremely high input resistance 10^{10} to $10^{15}\Omega$ for the MOSFET.

The metal of the gate terminal and the SC acts the parallel plates and the oxide layer acts as insulator of the state MOS capacitor. Between the drain and source terminal there is space for flow of carriers & it is called channel region. The voltage applied at the gate terminal is used to control the charge carriers in the channel i.e. drain current can be controlled using V_{GS} hence it is a voltage controlled device. There are two types of MOSFET

1) Depletion MOSFET
2) Enhancement MOSFET

3.13 DEPLETION MOSFET



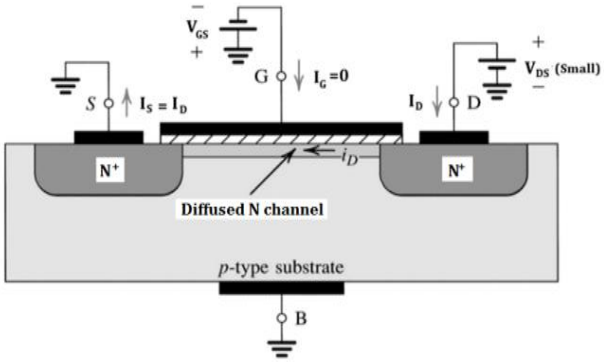


N-Channel P-Channel

In depletion MOSFET the conduction channel is physically implanted (rather than induced). Thus, for a depletion NMOS transistor, the channel conducts even if no gate to source voltage applied. Depending upon the polarity of applied Gate voltage with respect to source (V_{GS}), a depletion MOSFET operates in two modes

3.13.1 DEPLETION MODE

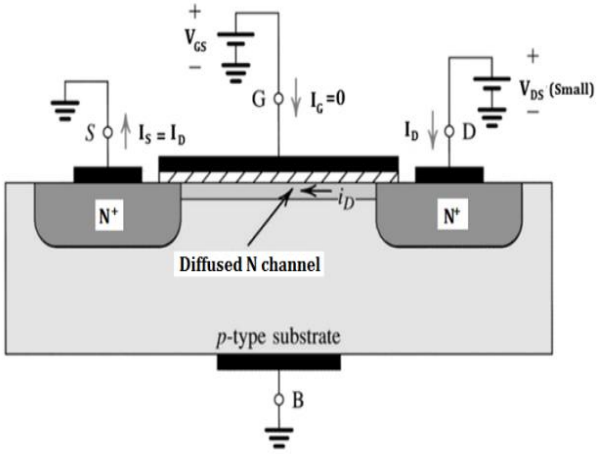
In depletion mode the applied V_{GS} decrease the majority charge carriers (electrons in N-MOS) in the channel. Due to applied V_{DS} an electric field induces in the channel & electrons flow from source to drain results in drain current.



1) When $V_{GS} = 0$ V , maximum no. of electrons flow from source to drain, hence drain current is maximum I_{DSS}.
2) When –veV_{GS} is applied, the holes from P-type substrate will be attracted in the channel (remember accumulation mode of MOS capacitor). Due to accumulation of holes the majority carriers in the channel (electrons) will recombine with the holes results in decrease in majority carrier concentration in the channel, hence drain current I_D decreases.
3) For a particular value of V_{GS} called $V_{GS(cut-off)}$, due to large no. of recombinations the majority carriers in the will be zero & hence drain current becomes zero.

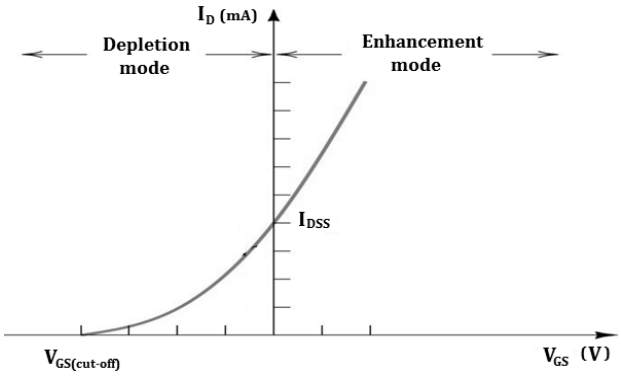
3.13.2 ENHANCEMENT MODE

In enhancement mode the applied V_{GS} increase the majority charge carriers (electrons in N-MOS) in the channel.

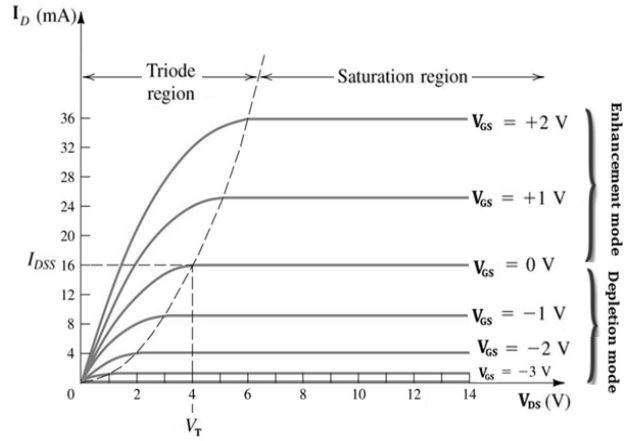


1) When $V_{GS} = 0$ V , minimum no. of electrons flow from source to drain, hence drain current is minimum I_{DSS}.
2) When positive $V_{GS} < V_T$ is applied, the electron concentration in the channel will not be affected i.e no inversion layer will form & same number of electrons will flow through channel & hence drain current remains minimum i.e. I_{DSS}.
3) When $V_{GS} \geq V_T$ is applied, the electrons in the p-type substrate will be attracted in the channel i.e. the majority carriers increases in the channel & hence drain current increases.

3.13.3 TRANSFER CHARACTERISTICS

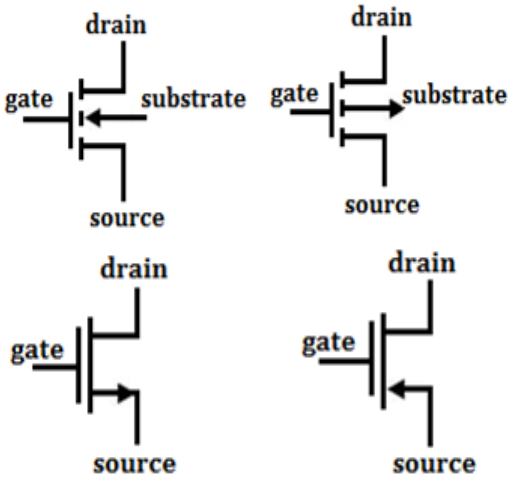


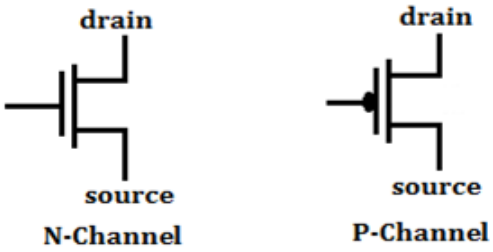
3.13.4 DRAIN CHARACTERISTICS



3.14 ENHANCEMENT MOSFET

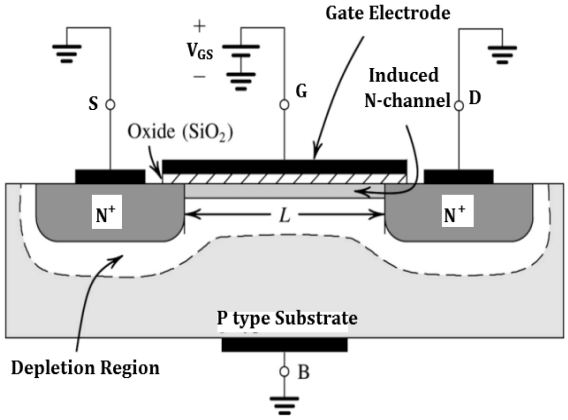
In enhancement MOSFET, also called a E-MOSFET, channel is absent between source & drain for conduction. When proper gate to source voltage is applied a channel is induced between source & drain. Also an Enhancement MOSFET operates only in enhancement mode.



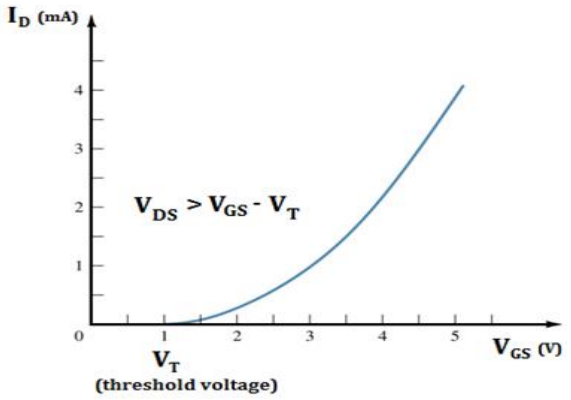


3.14.1 TRANSFER CHARACTERISTICS

(Varying V_{GS}& keeping V_{DS}constant)



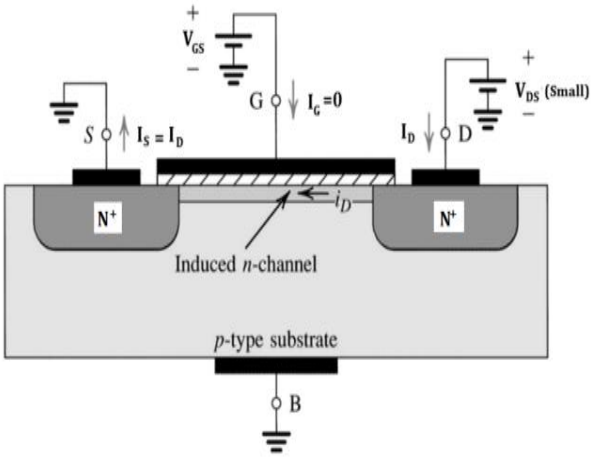
1) When $V_{GS} = 0$ V, the gate metal will be at zero volts & no channel will be induced & drain current $I_D$is 0.
2) When $V_{GS} < V_T$ (where V_T is called threshold voltage) is applied, again no channel will be induced &$I_D = 0$.
3) When $V_{GS} \geq V_T$is applied, the electrons in the P-type substrate will attracted towards oxide layer & an inversion layer is formed. This inversion layer of electrons acts as channel for N-channel enhancement MOSFET. With the creation of channel, MOSFET starts conducting & current $I_D$flows through device. With increase in V_{GS}more no of electrons are attracted in the channel & drain current increases.



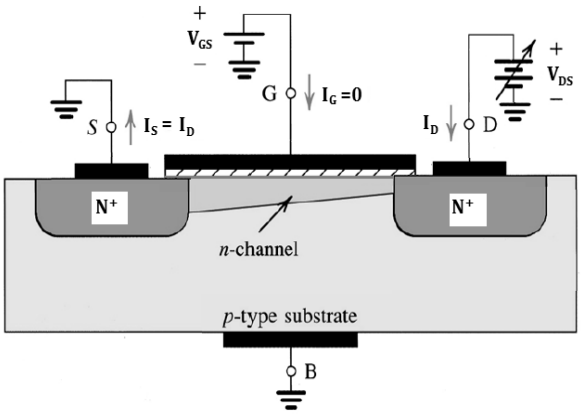
3.14.2 DRAIN CHARACTERISTICS

(Varying V_{DS} & keeping V_{GS} constant)

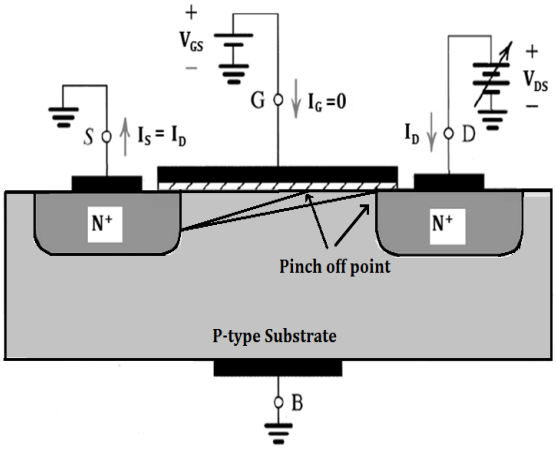
When proper gate to source voltage i.e. $V_{GS} \geq V_T$ is applied, a channel will induce & device starts conducting.



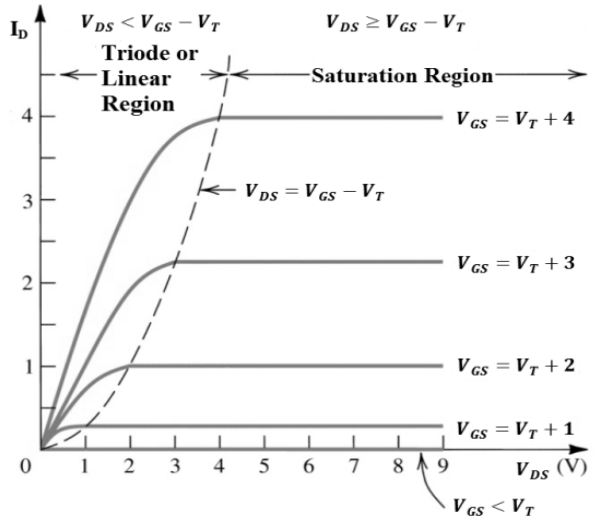
1) For small values of applied V_{DS}, the channel between source & drain is almost flat as shown in figure. With the application of V_{DS}, an electric is induced in the channel which directs from drain to source & this field is responsible for the flow of electrons in N-channel & hence drain current I_D.
2) With increase in V_{DS}, the reverse biasing of drain to body junction increases which results in penetration of depletion layer into channel & channel width gets tapered towards drain end as shown in figure below. With decrease in channel width the resistance of channel increases but at the same time field in the channel increases & the drain current increases linearly with applied V_{DS}.



3) When V_{DS} becomes $V_{DS(sat)} = V_{GS} - V_T$ (saturation voltage or overdrive voltage), the channel width reduces to zero i.e. channel is **pinched off** at drain end but due to a very strong electric field the charge carriers (electrons) are able to cross the depletion layer hence drain current continues to flow.
4) $V_{DS(sat)} > V_{GS} - V_T$, the pinch off point shifts towards source. This process where the length of channel can be varied with applied V_{DS} is called channel length modulation.



5) At $V_{DS} = V_{DS(sat)}$, the velocity of electrons almost saturates & hence for $V_{DS} \geq V_{DS(sat)}$ the drain current I_D remains constant.



3.14.3 OPERATING REGIONS

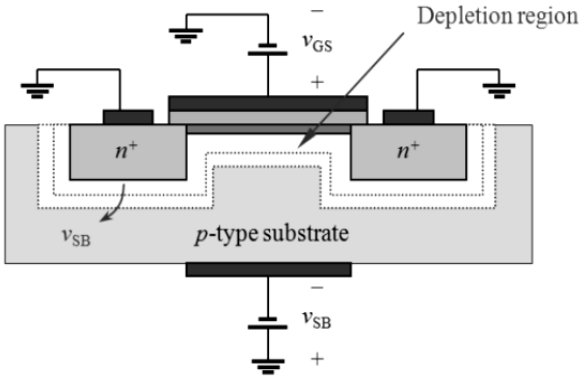
- **CUT-OFF**
  $V_{GS} < V_T$
  In cut-off no channel is induced & hence $I_D = 0$
- **TRIODE REGION**
  $V_{GS} \geq V_T \& V_{DS} < V_{DS(sat)}$
  In triode region I_D increases almost linearly with V_{DS}.
  $$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$$
- **SATURATION REGION**
  $V_{GS} \geq V_T \& V_{DS} \geq V_{DS(sat)}$
  In saturation region I_D is constant i.e. it is independent of V_{DS}.
  $$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)^2$$
  $$I_D = \frac{1}{2}K_n(V_{GS} - V_T)^2$$
  $$I_D \propto (V_{GS} - V_T)^2$$
  Where, $K_n = \mu_n C_{ox} \frac{W}{L}$ is called transconductance parameter

Note:

- In triode or ohmic region, a MOSFET can be used as voltage variable resistor (in linear region it follows Ohm's law like resistor & with change in V_{GS} we get another linear curve).
- In saturation region, a MOSFET can used as a voltage controlled constant current source (in saturation current I_D is almost constant & with change in V_{GS} we get another constant current curve).

3.14.4 BODY EFFECT

In MOSFET the source to body junction & drain to body junction must always be reverse biased in order to avoid conduction between S-B & D-B. In most of the cases source & body are connected together so that $V_{SB} = 0$ V i.e. no potential difference between source & body.
If source is biased at higher voltage than body i.e. $V_{SB} > 0$ V, the reverse biasing of source to body increases & the depletion layer width increases. This increase in depletion layer will make it difficult for applied V_{GS} to create a channel i.e. the threshold voltage V_T of MOSFET increases.



3.14.5 THRESHOLD VOLTAGE

- It is the minimum value of V_{GS} for which enhancement MOSFET enters into conduction. Therefore it should be as small as possible.
- V_T is positive for N-channel MOSFET & it is negative for P-channel MOSFET.
- Magnitude of V_T is around 1 V.
  $$V_T = V_{T0} + \gamma\left\{\sqrt{|2\varnothing_f + V_{SB}|} - \sqrt{|2\varnothing_f|}\right\}$$
  Where, V_{T0} is V_T when $V_{SB} = 0$
  $\gamma = \frac{\sqrt{2qN_A\varepsilon_{si}}}{C_{ox}}$ is called body effect parameter.

C_{ox} is oxide capacitance in F/m^2

$\varnothing_f = \frac{kT}{q} \ln \ln \frac{N_A}{n_i}$ a is called substrate Fermi potential.

N_A is doping concentration in P-type substrate

k is boltzmann's constant $\left(k = 8.62 \times 10^{-5} eV / {}^{o}K\right)$

$\varepsilon_{si} = \varepsilon_0 \varepsilon_{r(si)}$

n_i is intrinsic carrier concentration

V_{SB} is source to body voltage

Note: V_T decreases approximately by 2mV for 1^o rise in temperature.

3.14.6 PROCEDURE TO REDUCE V_T

1) **Choice of Gate Electrode:** Threshold voltage can be reduced by using N^+ doped poly silicon gate for N-channel MOSFET & P^+ doped poly silicon gate for P-channel MOSFET.
2) **Ion Implantation:** By implanting dopants through the gate conducting layer and gate insulating layer and deposit the dopants into the superficial portion of the substrate below the gate insulating layer.

3.15 COMPARISON BETWEEN MOSFET & JFET

1) Gate leakage current in MOSFET is of the order of 10^{-12}A, hence the input impedance is very high 10^{10} to 10^{15} Ω.
2) The drain characteristics of JFET are flatter than that of MOSFET, hence the drain resistance of JFET (0.1 to 1 M Ω) is much higher than that of MOSFET (1 to 50 K Ω).
3) As compared to JFET, MOSFETs are easier to fabricate

GATE QUESTIONS

Q.1 MOSFET can be used as a
a) Current controlled capacitor
b) Voltage controlled capacitor
c) Current controlled inductor
d) Voltage controlled inductor

[GATE-2001]

Q.2 The effective channel length of a MOSFET in saturation decreases with increase in
a) Gate voltage
b) Drain voltage
c) Source voltage
d) Body voltage

[GATE-2001]

Q.3 For an n-channel enhancement type MOSFET, if the source is connected at a higher potential than that of the bulk (i.e. V_{SB}> 0 volts), the threshold voltage V_T of the MOSFET will
a) Remain unchanged
b) Decrease
c) Change polarity
d) Increase

[GATE-2003]

Q.4 If for a silicon n-p-n transistor, the base to emitter voltage (V_{BE}) is 0.7 volts and the collector to base voltage (V_{CB}) is 0.2 volts, then the transistor is operating in the
a) Normal active mode
b) Saturation mode
c) Inverse active mode
d) Cutoff mode

[GATE-2004]

Q.5 Consider the following statements S1 and S2.
S1: The β of a bipolar transistor reduces if the base width is increased.
S2: The β of a bipolar transistor increases if the doping concentration in the base is increased. Which one of the following is correct?
a) S_1 is False and S_2 is TRUE
b) both S_1 and S_2 are TRUE
c)both S_1 and S_2 are FALSE
d) S_1 is TRUE and S_2 is FALSE

[GATE-2004]

Q.6 The phenomenon known as "Early Effect" in a bipolar transistor refers to a reduction of the effective base-width caused by
a) electron–hole recombination at the base
b) the reverse biasing of the base–collector junction
c) the forward biasing of emitter–bias junction
d) the early removal of stored base charge during saturation-to-cutoff switching

[GATE-2006]

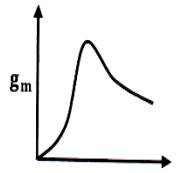
Q.7 The drain current of MOSFET in saturation is given by $I_D=K(V_{GS}-V_T)^2$ where K is a constant. The magnitude of the transconductance g_m is

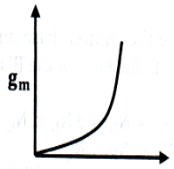
a) $\frac{K(V_{GS}-V_T)^2}{V_{DS}}$ b) $2K(V_{GS}-V_T)$

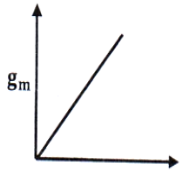
c) $\frac{I_d}{V_{GS}-V_{DS}}$ d) $\frac{K(V_{GS}-V_T)^2}{V_{GS}}$

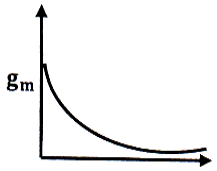
[GATE-2008]

Q.8 The measured transconductance g_m of an NOMS transistor operating in the linear region is plotted against the gate voltage V_G at a constant drain voltage V_D. Which of the following figures represents the expected dependence g_m on V_G?

a) 

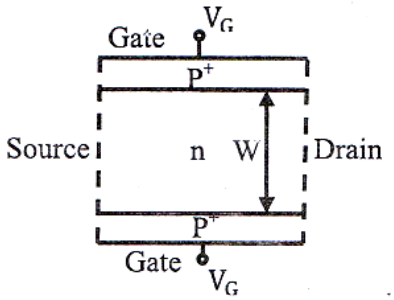
b) 

c) 

d) 

[GATE-2008]

Q.9 The cross section of a JFET is shown in the following figure. Let V_G be -2V and let V_p be the initial pinch-off voltage. If the width W is doubled (with other geometrical parameters and doping levels remaining the same), then the ratio between the mutual trans conductance's of the initial and the modified JFET is



a) 4

b) $\frac{1}{2}\left[\frac{1-\sqrt{2/V_p}}{1-\sqrt{1/(2V_p)}}\right]$

c) $\frac{1-\sqrt{2/V_p}}{1-\sqrt{1/(2V_p)}}$

d) $\frac{1-(2/\sqrt{V_p})}{1-(1/2\sqrt{V_p})}$

[GATE-2008]

Q.10 Consider the following two statements about the internal conditions in an n-channel MOSFET operating in the active region

S1:The inversion charge decrease from source to drain

S2:The channel potential increase from source to drain

Which of the following is correct?

a) Only S2 is true

b) Both S1 and S2 are false

c) Both S1 and S2 are true, but S2 is not a reason for S1

d) Both S1 and S2 are true, and S2 is a reason for S1

[GATE-2009]

Q.11 At room temperature, a possible value for the mobility of electrons in the inversion layer of a silicon n-channel MOSFET is

a) $450 cm^2/V\text{-}s$ b) $1350 cm^2/V\text{-}s$

c) $1800 cm^2/V\text{-}s$ d) $3600 cm^2/V\text{-}s$

[GATE-2010]

Q.12 In a uniformly doped BJT, assume that N_E, N_B and N_C are the emitter, base and collector doping in atoms / cm^3, respectively. If the emitter injection efficiency of the BJT is close to unity, which one of the following conditions is TRUE?

a) $N_E = N_B = N_C$

b) $N_E >> N_B$ and $N_B > N_C$

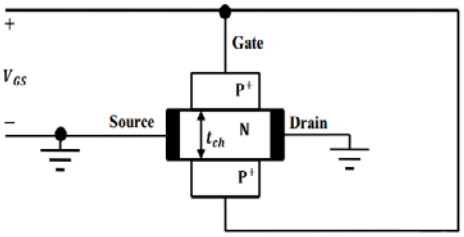
c) $N_E = N_B$ and $N_B < N_C$

d) $N_E < N_B < N_C$

[GATE-2010]

Common Data for Q.13 and Q.14

The channel resistance of an N- channel JFET shown in the figure below is 600 Ω when the full channel thickness (t_{ch}) of 10 μm is available for conduction. The built-in voltage of the gate P+N junction (V_{bi})is -1 .When the gate to source voltage (V_{GS}) is 0 V , the channel Is depleted by 1 μm on each side due to the built -in voltage and hence the thickness available for condition is only 8 μm



Q.13 The channel resistance when $V_{GS} = 0$Vis

a) 480 Ω b) 600 Ω
c) 750 Ω d) 1000 Ω

[GATE-2011]

Q.14 The channel resistance when $V_{GS} = -3$Vis

a) 360 Ω b) 917 Ω
c) 1000 Ω d) 3000 Ω

[GATE-2011]

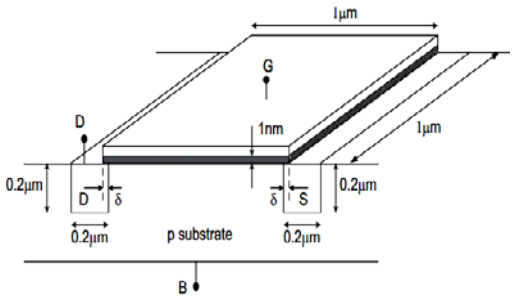
Q.15 The source of a silicon $\left(n_i = 10^{10} \text{percm}^3\right)$ n-channel MOS transistor has an area of 1 sq μm and a depth of 1 μm. If the dopant density in the source is $10^{19}/\text{cm}^3$, the number of holes in the source region with the above volume is approximately

a) 10^7 b) 100
c) 10 d) 0

[GATE-2011]

Common Data for Question 16 and 17

In the three dimensional view of a silicon n-channel MOS transistor shown below, δ=20 nm.The transistor is of width 1μm. The depletion width formed at every pn junction, is 10nm. The relative permittivity's of Si and O_2, respectively, are 11.7 and 3.9 and $\varepsilon_0 = 8.9\text{x}10^{-12}\,\text{F/m}$.



Q.16 The source body junction capacitance is approximately

a) 2 fF b) 7fF
c) 2pF d) 7 pF

[GATE-2012]

Q.17 The gate source overlap capacitance is approximately

a) 0.7fF b) 0.7pF
c) 0.35fF d) 0.24pF

[GATE-2012]

Q.18 If fixed positive charges are present in the gate oxide of an n-channel enhancement type MOSFET, it will lead to

a) a decrease in the threshold voltage
b) channel length modulation
c) an increase in substrate leakage current
d) an increase in accumulation capacitance

[GATE-2014-1]

Q.19 A BJT is biased in forward active mode, Assume V_{BE} = 0.7V, kT / q = 25mV and reverse saturation current $I_s = 10^{-13}$ A. The transconductance of the BJT (in mA/V) is _____.

[GATE-2014-1]

Q.20 A depletion type N-channel MOSFET is biased in its linear region for use as a voltage controlled resistor. Assume threshold voltage V_{TH} = 0.5V, V_{Gs} = 2.0V, V_{DS} = 5 V, W/L = 100, $C_{0x} = 10^{-8}\text{F/cm}^2$ and μ_n = 800 cm^2 /V — s. The value of the resistance of the voltage controlled resistor (in Ω) is_____.

[GATE-2014-1]

Q.21 An increase in the base recombination of a BJT will increase

a) the common emitter dc current gain β
b) the breakdown voltage BV_{CE0}
c) the unity-gain cut-off frequency f_T
d) the transconductance g_m

[GATE-14-2]

Q.22 In CMOS technology, shallow P-well or N-well regions can be formed using

a) low pressure chemical vapour deposition
b) low energy sputtering
c) low temperature dry oxidation
d) low energy ion-implantation

[GATE-2014-2]

Q.23 In MOSFET fabrication, the channel length is defined during the process of

a) Isolation oxide growth
b) Channel stop implantation
c) Poly-silicon gate patterning
d) Lithography step leading to the contact pads

[GATE-2014-3]

Q.24 The slope of the I_D vs V_{GS} curve of an n-channel MOSFET in linear regime is $10^{-3}\ \Omega^{-1}$ at V_{DS} = 0.1 V. For the same device, neglecting channel length modulation, the slope of the $\sqrt{I_D}$ vs V_{GS} curve (in $\sqrt{A}/V$) under saturation regime is approximately _____

[GATE-2014-3]

Q.25 An ideal MOS capacitor has boron doping-concentration of 10^{15} cm^{-3} in the substrate. When a gate voltage is applied, a depletion region of width 0.5 µm is formed with a surface (channel) potential of 0.2 V. Given that ε_o |= 8.854 x 10^{-14} F/cm and the relative permittivities of silicon and silicon dioxide are 12 and 4, respectively, the peak electric field (in V/ µm) in the oxide region is _____.

[GATE-2014-3]

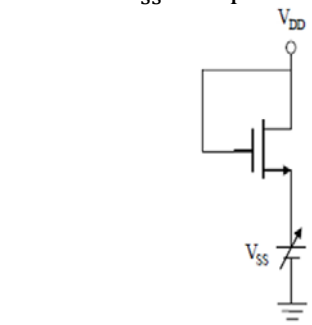
Q.26 Consider two BJTs biased at the same collector current with area $A_1 = 0.2\mu m \times 0.2\mu m$ and A_2 = 300µm x 300µm . Assuming that all other device parameters are identical, kT/q = 26 mV, the intrinsic carrier concentration is 1 x 10^{10} cm^{-3}, and q = 1.6 × 10^{-19} C, the difference between the base-emitter voltages (in mV) of the two BJTs (i.e., V_{BE1} — V_{BE2})is _____.

[GATE-2014-4]

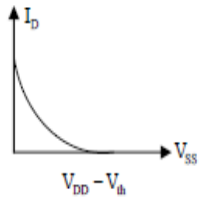
Q.27 A BJT in a common-base configuration is used to amplify a signal received by a 50Ω antenna. Assume kT/q = 25 mV. The value of the collector bias current (in mA) required to match the input impedance of the amplifier to the impedance of the antenna is _____.

[GATE-2014-4]

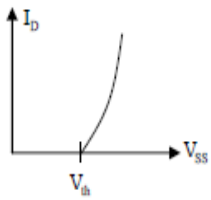
Q.28 For the NMOSFET in the circuit shown, the threshold voltage is V_{th}, where $V_{th} > 0$. The source voltage V_{ss} is varied from 0 to V_{DD} . Neglecting the channel length modulation, the drain current I_D as a function V_{ss} is represented by.



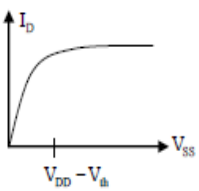
a)



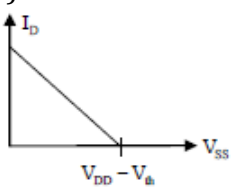
b)



c)



d)



[GATE-2015-1]

Q.29 A MOSFET in saturation has a drain current of lmA for V_{DS} = 0.5V . If the channel length modulation coefficient is 0.05 V^{-1}, the output resistance (in kΩ) of the MOSFET is _____.

[GATE-2015-1]

Q.30 In a MOS capacitor with an oxide layer thickness of 10 nm, the maximum depletion layer thickness is 100 nm. The permittivities of the semiconductor and the oxide layer are ε_s and ε_{ox} respectively. Assuming $\varepsilon_s/\varepsilon_{ox} = 3$, the ratio of the maximum capacitance to the minimum capacitance of this MOS capacitor is _____

[GATE-2015-2]

Q.31 Which one of the following processes is preferred to from the gate dielectric (SiO_2) of MOSFETs?

a)Sputtering
b) Molecular beam epitaxy
c) Wet oxidation
d) Dry oxidation

[GATE-2015-3]

Q.32 The current in an enhancement mode NMOS transistor biased in saturation mode was measured to be 1 mA at a drain-source voltage of 5 V. When the drain-source voltage was increased to 6 V while keeping gate-source voltage same, the drain current increased to 1.02 mA. Assume that drain to source saturation voltages is much smaller than the applied drain-source voltage. The channel length modulation parameter λ (in V^{-1}) is _____.

[GATE-2015-3]

Q.33 If the base width in a bipolar junction transistor is doubled, which one of the following statements will be TRUE?

a) Current gain will increase
b) Unity gain frequency will increase
c) Emitter base junction capacitance will increase
d) Early voltage will increase

[GATE-2015-3]

Q.34 An npn BJT having reverse saturation current $I_s = 10^{-15}$ A is biased in the forward active region with V_{BE} = 700 mV. The thermal voltage (V_T) is 25 mV and the current gain (β) may vary from 50 to 150 due to manufacturing variations. The maximum emitter current (in μA) is _____.

[GATE-2015-3]

Q.35 Consider the following statements for a metal oxide semiconductor field effect transistor (MOSFET):

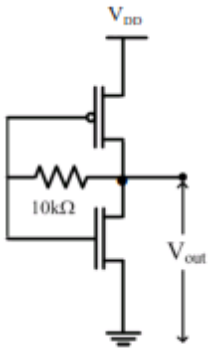
P: As channel length reduces, OFF-state current increases.
Q: As channel length reduces, output resistance increases.
R: As channel length reduces, threshold voltage remains constant.
S: As channel length reduces, ON current increases.

Which of the above statements are INCORRECT?

a) P and Q
b) P and S
c) Q and R
d) R and S

[GATE-2016-1]

Q.36 What is the voltage V_{out} in the following circuit?



a) 0V
b) $(|V_T \text{ of PMOS}| + V_T \text{ of NMOS})/2$
c) Switching threshold of inverter
d) V_{DD}

[GATE-2016-1]

Q.37 Consider an n-channel metal oxide semiconductor field effect transistor (MOSFET) with a gate-to source voltage of 1.8 V. Assume that $\frac{W}{L}=4$, $\mu_N C_{ox} = 70 \times 10^{-6} AV^{-2}$, the threshold voltage is 0.3V, and the channel length modulation parameter is 0.09 V^{-1}. In the saturation region, the drain conductance (in micro seimens) is _____.

[GATE-2016-1]

Q.38 A long-channel NMOS transistor is biased in the linear region with V_{DS} = 50mV and is used as a resistance. Which one of the following statements is NOT correct?

a) If the device width W is increased, the resistance decreases.
b) If the threshold voltage is reduced, the resistance decreases.
c) If the device length L is increased, the resistance increases.
d) If V_{GS} is increased, the resistance increases.

[GATE-2016-2]

Q.39 A voltage V_G is applied across a MOS capacitor with metal gate and p-type silicon substrate at T = 300K.The inversion carrier density (in number of carriers per unit area) for V_G = 0.8 V is 2×10^{11} cm^{-2}. For V_G = 1.3V, the inversion carrier density is 4×10^{11} cm^{-2}.What is the value of the inversion carrier density for V = 1.8 V?

a) 4.5×10^{11} cm^{-2}
b) 6.0×10^{11} cm^{-2}
c) 7.2×10^{11} cm^{-2}
d) 8.4×10^{11} cm^{-2}

[GATE-2016-2]

Q.40 The Ebers-Moll model of a BJT is valid

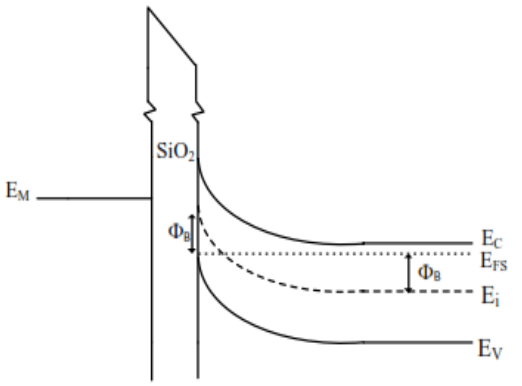
a) only in active mode
b) only in active and saturation modes
c) only in active and cut-off modes
d) in active, saturation and cut-off modes

[GATE-2016-2]

Q.41 Consider a long-channel NMOS transistor with source and body connected together. Assume that the electron mobility is independent of V_{GS} and V_{DS}. Given, g_m = 0.5 µA/V for V_{DS} = 50 mV and V_{GS}= 2 V, g_d = 8 µA/V for V_{GS} = 2 V and V_{DS} = 0 V, Where $g_m = \frac{\partial I_D}{\partial V_{GS}}$ and $g_d = \frac{\partial I_D}{\partial V_{DS}}$. The threshold voltage (in volts) of the transistor is _____.

[GATE-2016-2]

Q.42 The figure shows the band diagram of a Metal Oxide Semiconductor (MOS). The surface region of this MOS is in

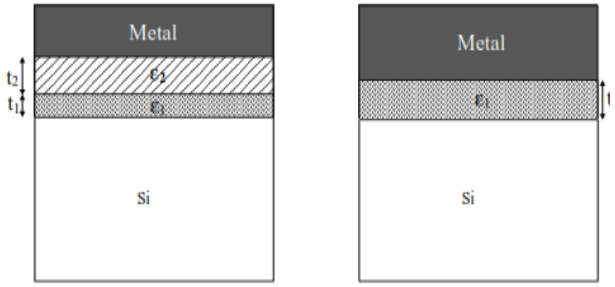


a) inversion
b) accumulation
c) depletion
d) flat band

[GATE-2016-2]

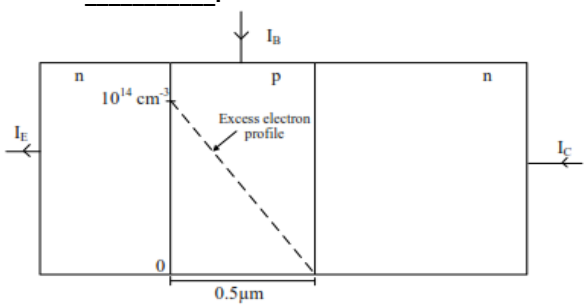
Q.43 Figures I and II show two MOS

capacitors of unit area. The capacitor in Figure I has insulator materials X (of thickness t_1 = 1 nm and dielectric constant ε_1 = 4) and Y (of thickness t_2 = 3 nm and dielectric constant ε_2 = 20). The capacitor in Figure II has only insulator material X of thickness t_{Eq}. If the capacitors are of equal capacitance, then the value of t_{Eq} (in nm) is _____.



[GATE-2016-3]

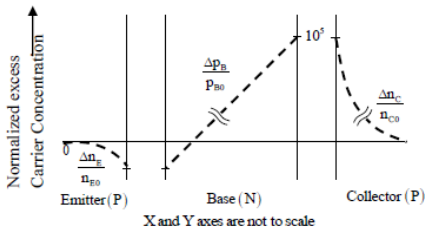
Q.44 The injected excess electron concentration profile in the base region of an npn BJT, biased in the active region, is linear, as shown in the figure. If the area of the emitter-base junction is 0.001 cm^2, μ_n = 800cm^2 /(V-s) in the base region and depletion layer widths are negligible, then the collector current I_C (in mA) at room temperature is _____.



(Given: thermal voltage V_T = 26 mV at room temperature, electronic charge q =1.6 × 10^{-19} C)

[GATE-2016-3]

Q.45 For a narrow base PNP BJT, the excess minority carrier concentration (Δn_E for emitter, Δp_B for base, Δn_C for collector) normalized to equilibrium minority carrier concentration (n_{E0} for emitter, p_{B0} for base, n_{C0} for collector) in the quasi-neutral emitter, base and collector regions are shown below. Which one of the following biasing modes is the transistor operating in?



a) Forward active b) Saturation

c) Inverse active d) Cutoff

[GATE-2017-1]

Q.46 An npn bipolar junction transistor (BJT) is operating in the active region. If the reverse bias across the base – collector junction is increased, then

a) the effective base width increases and common – emitter current gain increases
b) the effective base width increases and common – emitter current gain decreases
c) the effective base width decreases and common – emitter current gain increases
d) the effective base width decreases and common – emitter current gain decreases

[GATE-2017-2]

Q.47 Two n-channel MOSFETs, T1 and T2, are identical in all respects except that the width of T2 is double that of T1. Both the transistors are biased in the saturation region of operation, but the gate overdrive voltage (VGS-VTH) of T2 is double that of T1, where VGS and VTH are the gate – to – source voltage and threshold voltage of the transistors, respectively. If the drain current and transconductance of T1 are ID1 and gm1 respectively, the corresponding values of these two parameters for T2 are

a) $8I_{D1}$ and $2g_{m1}$

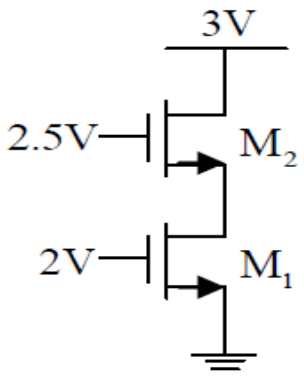
b) $8I_{D1}$ and $4g_{m1}$

c) $4I_{D1}$ and $4g_{m1}$

d) $4I_{D1}$ and $2g_{m1}$

[GATE-2017-2]

Q.48 Assuming that transistors M1 and M2 are identical and have a threshold voltage of 1V, the state of transistors M1 and M2 are respectively.



a) Saturation, Saturation
b) Linear, Linear
c) Linear, Saturation
d)Saturation,Linear

[GATE-2017-2]

ANSWER KEY:

1	2	3	4	5	6	7	8	9	10	11	12	13	14
(b)	(b)	(d)	(a)	(d)	(b)	(b)	(c)	(b)	(d)	(b)	(b)	(c)	(c)
15	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**	**26**	**27**	**28**
(d)	(a)	(a)	(a)	5.785	500	(b)	(d)	(c)	0.07	2.4	381	0.5	(a)
29	**30**	**31**	**32**	**33**	**34**	**35**	**36**	**37**	**38**	**39**	**40**	**41**	**42**
20	4.33	(d)	0.022	(d)	1475	(c)	(c)	28.47	(d)	(b)	(d)	1.2	(a)
43	**44**	**45**	**46**	**47**	**48**								
1.6	6.65	(c)	(b)	(b)	(c)								

EXPLANATIONS

Q.1 **(b)**
Voltage controlled capacitor.

Q.2 **(b)**
At the edge of saturation i.e. when drain to source voltage reaches $V_{D_{sat}}$ the inversion layer charge at the drain end becomes zero (ideally). The channel is said to be pinched off at the drain end. If the drain to source voltage V_{DS} is increased even further beyond the saturation edge so that $V_{DS} > V_{D_{sat}}$, an even larger portion of the channel becomes pinched off and effective channel length is reduced.

Q.3 **(d)**

$$V_T = V_{To} + \gamma\sqrt{\left|-2_{\Phi_F} + V_{SB}\right|} - \sqrt{\left|-2_{\Phi_F}\right|}$$

γ =substrate bias coefficient
V_{SB} =substrate bias voltage

Q.4 **(a)**
As $V_{BE} = 0.7$, i.e. positive, the base emitter junction of n-p-n transistor is forward biased& as $V_{CB} = 0.2V$ i.e. positive, collector base junction is reverse biased. Therefore the transistor is operating in normal active region.

Q.5 **(d)**

$$\beta = \frac{I_C}{I_B} = \frac{\alpha}{1-\alpha}$$

When base width increases, recombination in base region increases and **α** decreases & hence βdecreases.
If doping in base region increases, then recombination in base increases and α decreases thereby decreasing β.

Q.6 **(b)**
Early effect refers to a reduction of effective base width caused by the reverse bias of collector–base junction.

Q.7 **(b)**

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = 2K\left(V_{GS} - V_T\right)$$

Q.8 **(c)**
In linear region

$$I_D = K_n^{'}\frac{W}{L}\left[\left(V_{GS} - V_T\right)V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = K_n^{'}\frac{W}{L}V_{DS}$$

So
g_m remains constant with V_{GS}.
In saturation region

$$I_D = \frac{1}{2}K_n^{'}\frac{W}{L}\left(V_{GS} - V_{Th}\right)^2$$

$$g_m = K_n^{'}\frac{W}{L}\left(V_{GS} - V_{Th}\right)$$

Q.9 **(b)**

Q.10 **(d)**
From source to drain channel potential increases, so inversion charge reduces from source to drain.

Q.11 **(b)**
The mobility of electrons in Si is $1350cm^2 / V - sec$

Q.12 **(b)**
N_E ? $N_B$and$N_B > N_C$, for emitter injection efficiency of BJT close to unity.

Q.13 **(c)**

$$r_{don}\alpha\frac{1}{t_{Oh}}$$

At $V_{GS}=0, t_{Ch}=10\mu m$;
(Given r_d 600Ω)

$$r_d=\frac{10}{8}\times 600 \leftarrow \text{at} 8\mu m = 750\Omega$$

Q.14 (c)

Width of the depletion large W

$$\alpha\sqrt{V_{bi}+V_{GS}}$$

$$\frac{W_2}{W_1}=\sqrt{\frac{-1-3}{-1}}$$

$$\Rightarrow w_2=2w_1=2(1\mu m)=2\mu m$$

So that channel thickness

$$=10-4=6\mu m$$

$8\mu m - 750$

$6\mu m - ?$

$$r_d=\frac{8}{6}\times 750=1000\Omega$$

Q.15 (d)

$$n_i=10^{10}/cm^3 \text{ and } N_D=10^{19}/cm^3$$

$$\therefore P=\frac{n_i^2}{N_D}=10 as$$

So holes in volume v is = pV = 10^{-11}, since holes number cannot be a decimal number so $p = 0$

Q.16 (a)

Source body junction capacitor

$$C_j=\frac{\epsilon A}{d}=\frac{\epsilon_0\epsilon_r A}{d}$$

Here $\epsilon_r = 11.7$ as there is Si capacitor

$$A=1\mu m\times 0.2\mu m=0.2\times 10^{-12}\ m^2$$

d =depletion width of p-n junction

$d = 10mm = 10^{-8}m$

so

$$C_j=\frac{8.9\times10^{-12}\times11.7\times0.2\times10^{-12}}{10^{-8}}$$

$$C_j=2.082\times10^{-15}F$$

$$C_j=2fF$$

Q.17 (a)

Gate source capacitance C_g is

$$C_g=\frac{\epsilon_1 A_1}{d_1}=\frac{\epsilon_0\epsilon_{r1}A_1}{d_1}$$

$\epsilon_{r1} = 3.9$as between gate and source there is SiO_2

$$A_1=1\mu m\times\delta$$

$$=1\times10^{-6}\times20\times10^{-9}$$

$$=2\times10^{-14}m^2$$

$d_1 = 1\ nm = 10^{-9}m$

So

$$C_g=\frac{8.9\times10^{-12}\times3.9\times2\times10^{-14}}{10^{-9}}$$

$$C_g=69.42\times10^{-17}F$$

$$C_g=0.69\times10^{-15}$$

$$C_g=0.7fF$$

Q.18 (a)

Q.19 (5.785)

V_{BE} = 0.7V, $\frac{KT}{q}$ = 25 mV, $I_s = 10^{-13}$

Transconductance, $g_m = \frac{I_C}{V_T}$

$I_C = Is\ [e^{V_{BE}/V_T} - 1]$

$=10^{-13}\ [e^{0.7/25mV} - 1] = 144.625$ mA

$$\therefore g_m=\frac{I_C}{V_T}=\frac{144.625mA}{25mV}$$

=5.785 A /V

Q.20 (500)

Given V_T = -0.5V; V_{GS}= 2V,

V_{DS} = 5 V: $W/_L$ =100;

$C_{\theta_x}=10^{-8}$ f / cm

μ_n =800 cm^2 / v - s

$$I_D=\frac{1}{2}\mu_n C_0\times\frac{W}{L}\left[2(V_{GS}-V_T)V_{DS}-V_{DS}^2\right]$$

$$\left[\frac{\partial I_D}{\partial V_{DS}}\right]^{-1}=r_{ds}$$

$$\left[\frac{\partial}{\partial V_{DS}}\left\{\frac{1}{2}\mu_n C_{0x}\frac{W}{L}\left[2(V_{GS}-V_T)V_{DS}-V_{DS}^2\right]\right\}\right]^{-1}$$

$$=[\mu_n C_{0x}\frac{W}{L}(V_{GS}-V_T)-\mu_n C_{0x}\frac{W}{L}V_{DS}]^{-1}a$$

$$\Rightarrow |r_{ds}| = \left| \frac{1}{\mu_n C_{0x} \frac{W}{L}(V_{GS} - V_T - V_{DS}} \right|$$

$$= \left| \frac{1}{800 \times 10^{-8} \times 100(2 + 0.5 - 5)} \right| = 500\Omega$$

Q.21 (B)

Q.22 (D)

Q.23 (C)

Q.24 (0.07)

In linear region,

$$I_D = k\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$$\frac{\partial I_D}{\partial V_{GS}} = 10^{-3} = kV_{DS}$$

$\therefore V_{DS}$ is small. $\frac{V_{DS^2}}{2}$ neglected

$$\Rightarrow K = \frac{10^{-3}}{0.1} = 0.01$$

In Saturation region ,

$$I_D = \frac{1}{2}k(V_{GS} - V_T)^2$$

$$\sqrt{I_D} = \sqrt{\frac{k}{2}}(V_{GS} - V_T)$$

$$\frac{\partial\sqrt{I_D}}{\partial V_{GS}} = \sqrt{\frac{k}{2}} = \sqrt{\frac{0.01}{2}} = 0.07$$

Q.25 (2.4)

$$E_s = \frac{2 \times 0.2}{0.5} = 0.8v/\mu m$$

$$E_{ox} = \frac{E_s}{E_{ox}}E_s = 2.4v/\mu m$$

Q.26 (381)

$I_{C_1} = I_{C_2}$ (Given)

$$I_{S1}e^{\frac{V_{BE1}}{V_T}} = I_{S2}e^{V_{BE2}/V_T}$$

$$e^{(V_{BE1} - V_{BE2})/V_T} = \frac{I_{S2}}{I_{S1}}$$

$$V_{BE1} - V_{BE2} = V_T \ln\frac{I_{S2}}{I_{S1}}$$

$$= 26 \times 10^{-3}\ln\left[\frac{300 \times 300}{0.2 \times 0.2}\right]$$

$\because I_S \alpha A(V_{BE1} - V_{BE2}) = 381mV$

Q.27 (0.5)

Input impedance of CB amplifier,

$$z_i = r_e = \frac{V_I}{I_E}$$

$$\Rightarrow 50 = \frac{25mV}{I_E}$$ ($\because$signal is received from 50Ω antenna and V_T= 25 mV)

$$\Rightarrow I_E = \frac{25m\ V}{50\Omega} = 0.5mA$$

Q.28 (a)

$V_{GS} = V_{DS}$

Hence MOS Transistor is in saturation.

In saturation,

$$I_D = k(V_{GS} - V_r)^2 = k(V_{DD} - V_{ss} - V_T)^2$$

As $V_{ss} \uparrow$ $I_D \downarrow$ (Not linearly because square factor)

Hence option (a) correct

Q.29 (20)

Under channel length modulation

$$I_D = I_{Dsat}(1+\lambda V_{DS})$$

$$\frac{dI_D}{dV_{DS}} = \frac{1}{r_0} = \lambda I_{Dsat}$$

$$r_0 = \frac{1}{\lambda I_{Dsat}} = \frac{1}{0.05 \times 10^{-3}}$$

$= 20\ k\Omega$

Q.30 (4.33)

$$\frac{C_{max}}{C_{min}} = \frac{\frac{\epsilon_{ox}}{t_{ox}}}{\frac{\frac{\epsilon_{ox}}{t_{ox}} \times \frac{\epsilon_s}{X_{dmax}}}{\frac{\epsilon_{ox}}{t_{ox}} + \frac{\epsilon_s}{X_{dmax}}}}$$

$$= \left[1 + \frac{X_{dmax}}{t_{ox}} \times \frac{\epsilon_{ox}}{\epsilon_x}\right]$$

$$=\left[1+\frac{100}{10}\times\frac{1}{3}\right]=4.33$$

Q.31 (d)

Q.32 (0.022)

NMOS SATURATION

$I_D = 1mA@V_{DS} = 5V$

$I_D = 1.02mA@V_{DS} = 6V$

$V_{DSat} = V_{DS}$

$I_D = k(V_{GS} - V_T)^2(1+\lambda V_{DS})$

$I_D = k'(1+\lambda V_{DS})$

$10^{-3} = k'(1+\lambda 5)$

$1.02\times10^{-3} = k'(1+6\lambda)$

$1.02=\frac{1+6\lambda}{1+5\lambda} \Rightarrow 1.02+5.1\lambda = 1+6\lambda$

$0.02 = 0.9\lambda$

$\lambda = 0.022V^{-1}$

Q.33 (d)

W_B doubled (increased) → early effect is still present but its effect less severe relative to previous W_B. Slope I_c Vs V_{CE} decreases

Q.34 (1475)

$$I_B = \frac{I_C}{\beta} = \frac{I_s}{\beta}e^{V_{BE}/V_T}$$

$$I_E = (\beta+1)I_B$$

$$= \frac{\beta+1}{\beta}I_s.e^{V_{BE}/V_T}a$$

$$=(1.02)(10^{-9}\times10^{-6})e^{\frac{700\times10^{-3}}{25\times10^{-3}}}$$

= 1475 μA

Q.35 (c)

$$\rightarrow I\infty\frac{1}{L} \text{ so } L\downarrow I_{OFF}\uparrow$$

$$\rightarrow r_d = \frac{\partial V_{DS}}{\partial I_D} = \frac{L}{\mu_n C_{ox} W(V_{us} - V_t - V_{DS})}$$

So $L\downarrow r_d\downarrow$

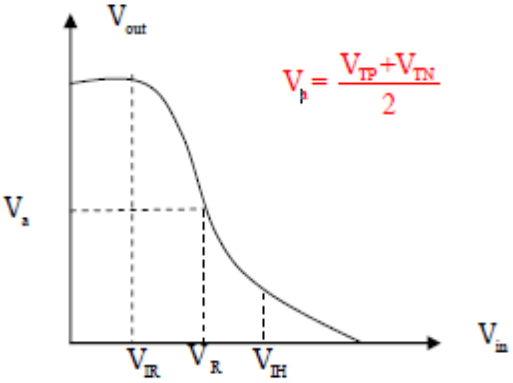
→if the channel length reduces, then threshold voltage also changes

$L\downarrow I_{ON}\downarrow$

So option (C) is matching

Q.36 (c)

The transfer characteristics of the CMOS inverter is as follows



Since the inverter is connected in feedback loop formed by connecting 10XΩ resistor between the output and input, the output goes and stays at the middle of the characteristics

$$V_a = \frac{V_{IR}+V_{IH}}{2}$$

$V_a \Rightarrow$ Switching threshold of inverter

Q.37 (28.47)

$$I_{DS} = \frac{1}{2}\mu_N C_{ox}\frac{W}{L}(V_{GS}-V_T)^2(1+\lambda V_{DS})$$

$$g_{ds} = \frac{dI_{DS}}{dV_{DS}} = \lambda\frac{1}{2}\mu_n C_0\times\frac{W}{L}(V_{GS}-V_T)^2$$

$$= 0.09\times0.5\times70\times10^{-6}\times4(1.8-0.3)^2$$

=28.47 μs

Q.38 (d)

$$R_{on} = \frac{1}{k_n(V_{GS}-V_t)}$$

$$k_n = \mu_n c_{ox}.\frac{W}{L}$$

$$\text{So, } R_{on} = \frac{L}{\mu_n c_{ox} W(V_{GS}-V_t)}$$

Q.39 (b)

$Q_{inv} = k(V_{GS}-V_t), V_{GS} > V_t$

$|Q_{inv}| = qN_i$

$qN_i = k(V_{GS} - V_t)$

Given

Case (i)

$q(2\times 10^{11}\ cm^{-2}) = k(0.8 - V_t)$

Case (ii)

$q(4\times 10^{11}\ cm^{-2}) = k(1.3 - V_t)$

$2 = \dfrac{1.3 - V_t}{0.8 - V_t}$

$1.6 - 2V_t = 1.3 - V_t$

$V_t = 0.3$

So, $k = \dfrac{2\times 10^{11}}{0.5}\times 1.6\times 10^{-19}$

So,

$1.6\times 10^{-19}\times N_i = 4\times 10^{11}\times 1.6\times 10^{-19}(1.5)$

$N_i = 6\times 10^{11}\ cm^{-2}$

Q.40 (d)

Q.41 (1.2)

From given conditions

$V_{DS} \le V_{GS} - V_t$,

So transistor is linear

$$I_D = k_n\left[(V_{GS} - V_t)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$$\frac{\partial I_D}{\partial V_{GS}} = k_n.V_{DS}$$

$$k_n = \frac{0.5\times 10^{-6}}{50\times 10^{-3}} = \frac{1}{100}\times 10^{-3} = 10^{-5}\ A/v^2$$

$$\text{So, } \frac{\partial I_D}{V_{DS}} = k_n.(V_{GS} - V_t)$$

$$8\times 10^{-6} = 10^{-5}[2 - V_t]$$

$$V_t = 2 - 0.8 = 1.2V$$

Q.42 (a)

The semiconductor used in the MOSFET is n-type. At the surface the intrinsic level is above E_F as it is found at the distance of below E_F, So, the surface is in inversion region.

Q.43 (1.6)

$$C_I = \frac{\frac{E_1}{t_1}.\frac{E_2}{t_2}}{\frac{E_1}{t_1} + \frac{E_2}{t_2}}$$

$$= \frac{E_1E_2}{E_1t_2 + E_2t_1}$$

$$= \frac{4\times 20}{(4\times 2) + (20\times 1)} = 2.5$$

$$C_{II} = \frac{E_1}{t_{Eq}} \Rightarrow \frac{4}{t_{Eq}} = 2.5 \Rightarrow t_{Eq} = 1.6nm$$

Q.44 (6.65)

$$|I_c| \approx qAD_n\frac{dn}{dx}$$

$$= qA\mu_nV_t\frac{dn}{dx}$$

$$= 1.6\times 10^{-19}\times 0.001\times 800\times 26\times 10^{-3}\left(\frac{10^{14} - 0}{0.5\times 10^{-4}}\right)$$

$$|I_c| = 6.65mA$$

Q.45 (c)

As per the change carrier profile, base – to – emitter junction is reverse bias and base to collector junction is forward bias, so it works in Inverse active.

Q.46 (c)

If the reverse bias voltage across the base collector junction is increased, then their effective base width will decrease and collector current will increase, therefore their common-emitter current gain increases.

Q.47 (b)

Drain current in saturation is

$$I_D = \frac{1}{2}\mu_nC_{OX}\frac{W}{L}[V_{GS} - V_{TH}]^2$$

For transmitter T_1

$$I_D = I_{D1}$$

$$g_m = g_{m1} = \frac{\partial I_{D1}}{\partial V_{GS}}$$

$$= \mu_n C_{OX} \frac{\omega}{L}\left(V_{GS} - V_{TH}\right)$$

For transmitter T_2

$$W_2 = 2W_1 = 2W$$

$$\left(V_{GS} - V_{TH}\right)_2 = 2\left(V_{GS} - V_{TH}\right)_1$$

$$= 2\left(V_{GS} - V_{TH}\right)$$

$$I_{D2} = \frac{1}{2}\mu_n C_{OX} \frac{2W}{L}\left[2\left(V_{GS} - V_{TH}\right)\right]^2$$

$$= 8I_{D2}$$

$$g_{m2} = \frac{\partial I_{D2}}{\partial V_{GS2}}$$

$$= \mu_n C_{OX} \frac{2W}{L} x 2\left(V_{GS} - V_{TH}\right)$$

$$= 4g_{m1}$$

Q.48 (c)

If $V_D \geq V_G - V_{TH}$, then the transistor is working in saturation region

So for M_2 transistor

$$V_{D2} > V_{G2} - V_{TH}$$

$$3V > \left(2.5 - 1\right)V$$

Assume that M_1 is working in saturation, so that

$$I_{D1} = I_{D2}$$

$$V_{GS1} - V_{TH} = V_{GS2} - V_{TH}$$

$$2V = V_{G2} - V_{S2}$$

$$= 2.5V - V_{S2}$$

$$\therefore V_{S2} = V_{D1} = 0.5V$$

Now for M_1 transistor to work in saturation $V_{D1} \geq V_{G1} - V_{TH}$,but it is not satisfied by M_1 transistor and $V_{G1} > V_{TH}$, so transistor M_1 is ON but working in linear region.

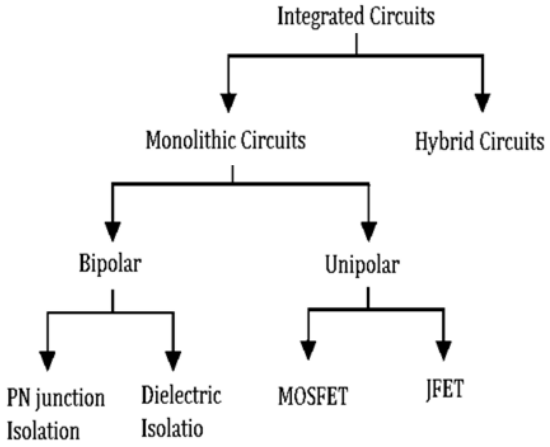
4 IC FABRICATION

4.1 CLASSIFICATION

Integrated circuits offer a wide range of applications and could be broadly classified as:

1) Digital ICs
2) Linear ICs

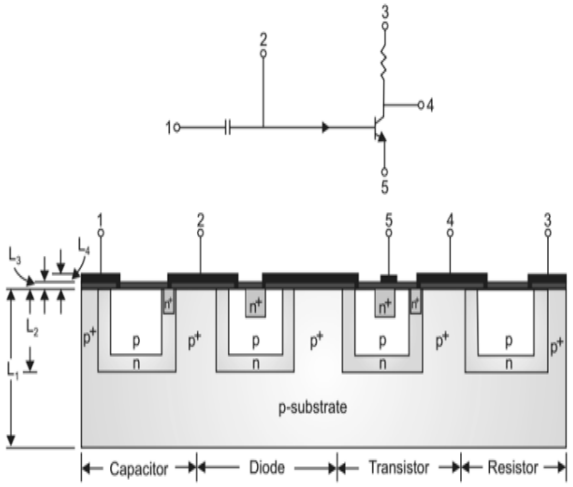
Based upon the requirements, two distinctly different IC technologies namely, Monolithic technology and Hybrid technology have been developed. In monolithic integrated circuits, all circuit components, both active and passive elements and their interconnections are manufactured into or on top of a single chip of silicon. In hybrid circuits, separate component parts are attached to a ceramic substrate and interconnected by means of either metallization pattern or wire bonds.



4.2 MONOLITHIC IC TECHNOLOGY

A monolithic circuit means a circuit fabricated from a single stone or a single crystal. The origin of the word 'monolithic' is from the Greek word moons meaning 'single' and litho meaning 'stone'. So monolithic integrated circuits are, in fact, made in a single piece of single crystal silicon.

A standard 10 cm diameter wafer can be divided into approximately 8000 rectangular chips of sides 1 mm. Each IC chip may contain as few as tens of components to several thousand components. The fabrication of discrete devices such as transistor, diode or an integrated circuit in general can be done by the same technology. The various processes usually take place through a single plane and therefore, the technology is referred to as planar technology. A simple circuit, when fabricated by silicon planar technology will have the cross sectional view shown in Fig.



Complete cross sectional view when circuit is transformed into monolithic form

An IC in general, consists of four distinct layers, as follows:

Layer No. 1 (~ 400 μm) is a p-type silicon substrate upon which the integrated circuit is fabricated.

Layer No. 2 (~ 5–25 μm) is a thin n-type material grown as a single crystal extension of the substrate using epitaxial deposition technique. All active and passive components are fabricated within this layer using selective diffusion of impurities.

Layer No. 3 (0.02–2μm) is a very thin S_iO_2 layer for preventing diffusion of impurities wherever not required using photolithographic technique.

Layer No. 4 (~ 1μm) is an aluminium layer used for obtaining interconnection between components.

4.3 BASIC PLANER PROCESS

The basic processes used to fabricate ICs using silicon planar technology can be categorized as follows:

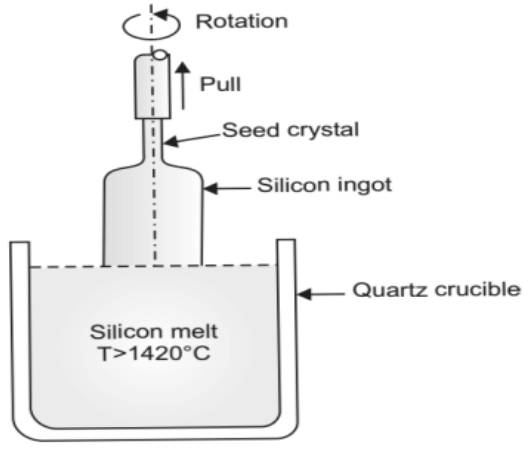
1) Silicon wafer (substrate) preparation
2) Epitaxial growth
3) Oxidation
4) Photolithography
5) X ray & electron beam lithography
6) Diffusion
7) Ion implantation
8) Isolation techniques
9) Metallization
10) Assembly processing and packaging

4.3.1 SILICON WAFER PREPARATION

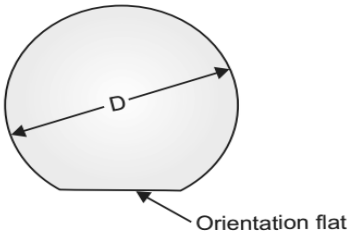
The following steps are used in the preparation of Si-wafers:

1) Crystal growth and doping
2) Ingot trimming and grinding
3) Ingot slicing
4) Wafer polishing and etching
5) Wafer cleaning

The starting material for crystal growth is highly purified (99.99999) polycrystalline silicon. The Czochralski crystal growth process is the most often used for producing single crystal silicon ingots. The polycrystalline silicon together with an appropriate amount of dopant is put in a quartz crucible and is then placed in a furnace. The material is then heated to a temperature in excess of the silicon melting point of 1420°C. A small single crystal rod of silicon called a seed crystal is then dipped into the silicon-melt and slowly pulled out as shown in Fig. 1.5. As the seed crystal is pulled out of the melt, it brings with it a solidified mass of silicon with the same crystalline structure as that of seed crystal. During the crystal pulling process, the seed crystal and the crucible are rotated in opposite directions in order to produce ingots of circular cross-section. The diameter of the ingot is controlled by the pulling rate and the melt temperature. Ingot diameter of about 10 to 15 cm is common and ingot length is generally of the order of 100 cm. Next the top and bottom portions of the ingot are cut off and the ingot surface is ground to produce an exact diameter (D = 10, 12.5, 15 cm). The ingot is also ground flat slightly along the length to get a reference plane. The ingot is then sliced using a stainless steel saw blade with industrial diamonds embedded into the inner diameter cutting edge. This produces circular wafers or slices as shown in figure. The orientation flat portion serves as a useful reference plane for the various processes described later. The silicon wafers so obtained have very rough surface due to slicing operation. These wafers undergo a number of polishing steps to produce a flat surface. Then one side of the wafer is given a final mirror-smooth highly polished finish, whereas the other side is simply lapped on an abrasive lapping machine to obtain an acceptable degree of flatness. Finally, the wafers are thoroughly rinsed and dried. A raw cut slice of thickness 23-40 mils produces wafers of 16–32 mils thickness after all the polishing steps. These silicon wafers will contain several hundred rectangular chips, each one containing a complete integrated circuit.



Czochralski crystal growth



Silicon wafer, D = 10, 12.5, 15 cm showing flat orientation

After all the IC fabrication processes are complete, these wafers are sawed into 100 to 8000 rectangular chips having side of 10 to 1 mm. Each chip is a single IC and may contain hundreds of components. The wafer thickness therefore is so chosen that it is possible to separate chips without breaking and at the same time, it gives sufficient mechanical strength to the IC chip.

4.3.2 EPITAXIAL GROWTH

The word epitaxial is derived from Greek word epic meaning 'upon' and the past tense of the word Tenino meaning 'arranged'. So, one could describe epitaxial as, arranging atoms in single crystal fashion upon a single crystal substrate, so that the resulting layer is an extension of the substrate crystal structure. The basic chemical reaction used for the epitaxial growth of pure silicon is the hydrogen reduction of silicon tetrachloride.

$$SiCl_4 + 2H_2 1200°C Si + 4HCl$$

Mostly, epitaxial films with specific impurity concentration are required. This is accomplished by introducing phosphine (PH_3) for the n-type and bi-borne (B_2H_6) for p-type doping into the silicon-tetrachloride hydrogen gas stream. The process is carried out in a reaction chamber consisting of a long cylindrical quartz tube encircled by an RF induction coil. Figure 1.7 shows the diagrammatic representation of the system used. The silicon wafers are placed on a rectangular graphite rod called a boat.

This boat is then placed in the reaction chamber where the graphite is heated inductively to a temperature 1200°C. The various gases required for the growth of desired epitaxial layers are introduced into the system through a control console.

4.3.3 OXIDATION

SiO2 has the property of preventing the diffusion of almost all impurities through it. It serves two very important purposes.

1. SiO2 is an extremely hard protective coating and is unaffected by almost all re-agents except hydrofluoric acid. Thus, it stands against any contamination.
2. By selective etching SiO2, diffusion of impurities through carefully defined windows in the SiO2 can be accomplished to fabricate various components.

The silicon wafers are stacked up in a quartz boat and then inserted into quartz furnace tube. The Si-wafers are raised to a high temperature in the range of 950 to 1115°C and at the same time, exposed to a gas containing O2 or H2O or both. The chemical reaction is

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2$$

This oxidation process is called thermal oxidation because high temperature is used to grow the oxide layer. The thickness of the film is governed by time, temperature and the moisture content. The thickness of oxide layer is usually in the order of 0.02 to 2 μm.

4.3.4 PHOTOLITHOGRAPHY

With the help of photolithography, it has become possible to produce microscopically small circuit and device patterns on Si-wafers. As many as 10,000 transistors can be fabricated on a 1 cm × 1 cm chip. The conventional photolithographic process uses ultraviolet light exposure and device dimension or line width as small as 2 mm can be obtained. However, with the advent of latest technology using X-ray or electron beam lithographic techniques, it has become

possible to produce device dimension down to sub-micron range (<1 μ m). Photolithography involves two processes, namely:

1) Making of a photographic mask
2) Photo etching

The making of a photographic mask involves the following sequence of operations—first the preparation of initial artwork and secondly, its reduction. The initial layout or artwork of an IC is normally done at a scale several hundred times larger than the final dimensions of the finished monolithic circuit. This is because, for a tiny chip, larger the artwork, more accurate is the final mask. For example, it is often required to make an opening of width about 1 mil (25 μm). Obviously, this cannot be managed by any draftsman even with his thinnest of sketch pens. So the drawings are made magnified and often by a factor of 500. With this magnification, it is easy to see that a width of one mil is magnified to a width of 500 mils, that is, about 1.2 cm. Therefore, for a finished monolithic chip of area 50 mils × 50 mils, the artwork will be made on an area of about 60 cm × 60 cm.

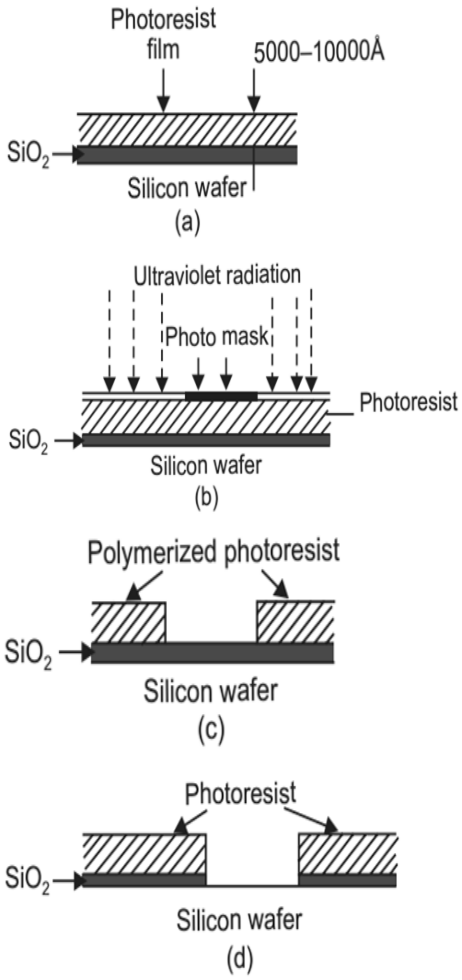
This initial layout is then decomposed into several mask layers, each corresponding to a process step in the fabrication schedule, e.g., a mask for base diffusion, another for collector diffusion, another for metallization and so on.

For photographic purpose, artwork should not contain any line drawings but must be of alternate clear and opaque regions. This is accomplished by the use of clear Mylar coated with a sheet of red photographically opaque Mylar (trade name-Rubylith). The red layer can be easily peeled off thus exposing clear areas with a knife edge from the regions where impurities have to be diffused. The artwork is usually produced on a precision drafting machine, known as coordinatograph. The coordinatograph has a cutting head that can be positioned accurately and moved along two perpendicular axes. The coordinatograph outlines the pattern cutting through the red mylar without damaging the clear layer underneath.

This rubylith pattern of individual mask is photographed and then reduced in steps by a factor of 5 or 10 several times to finally obtain the exact image size. The final image also must be repeated many times in a matrix array, so that many ICs will be produced in one process. The photo repeating is done with a step and repeat camera. This is an imaging device with a photographic plate on a movable platform. Between exposures, the plate is moved in equal steps so that successive images form in an array. When the exposed plate is developed, it becomes a master mask. The masks, actually used in IC processing are made by contact printing from the master. These working masks wear out with use and are replaced as required.

Photo-etching is used for the removal of SiO_2 from desired regions so that the desired impurities can be diffused. The wafer is coated with a film of photosensitive emulsion (Kodak Photoresist KPR). The thickness of the film is in the range of 5000–10000 Å as shown in fig. (a). The mask negative of the desired pattern) as prepared by steps described earlier is placed over the photoresist coated wafer as shown in Fig. (b). This is now exposed to ultraviolet light, so that KPR becomes polymerized beneath the transparent regions of the mask. The mask is then removed and the wafer is developed using a chemical (trichloroethylene) which dissolves the unexposed/unpolymerized regions on the photoresist and leaves the pattern as shown in fig. (c). The polymerized photoresist is next fixed or cured, so that it becomes immune to certain chemicals called etchants used in subsequent processing steps. The chip is immersed in the etching solution of hydrofluoric acid, which removes the SiO_2 from the areas which are not protected by KPR as shown in fig.(d). After diffusion of impurities, the photoresist is removed with

a chemical solvent (hot H_2SO_4) and mechanical abrasion.
The etching process described is a wet etching process and the chemical reagents used are in liquid form. A new process used these days is a dry etching process called plasma etching. A major advantage of the dry etching process is that it is possible to achieve smaller line openings ($\leq 1\mu m$) compared to wet process.

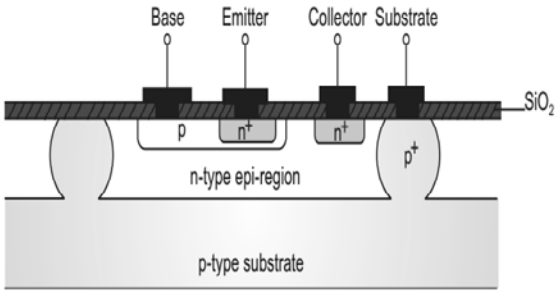


4.3.5 XRAY & ELECTRON BEAM LITHOGRAPHY

With conventional ultraviolet (UV) photolithography process in which the UV wavelengths used are in the range, 0.3 to 0.4 μm, the minimum device dimensions or line widths limited by diffraction effects to around five wavelengths or about 2 μm. This is what puts an upper limit on the IC device density using UV photolithography.
With the advent of X-ray and electron beam lithography techniques, it has become possible to produce device dimensions down to submicron range ($< 1\mu m$). This is due to much shorter wavelengths involved. With these techniques, MOSFET with gate length as small as 0.25 μm have been made.

4.3.6 DIFFUSION

Another important process in the fabrication of monolithic ICs is the diffusion of impurities in the silicon chip. This uses a high temperature furnace having a flat temperature profile over a useful length (about 20" length). A quartz boat containing about 20 cleaned wafers is pushed into the hot zone with temperature maintained at about a 1000°C. Impurities to be diffused are rarely used in their elemental forms. Normally, compounds such as B_2O_3 (Boron oxide), BCl_3 (Boron chloride) are used for Boron and P_2O_5 (Phosphorous pentaoxide) and $POCl_3$ (Phosphorous oxychloride) are used as sources of Phosphorous. A carrier gas, such as dry oxygen or nitrogen is normally used for sweeping the impurity to the high temperature zone. The depth of diffusion depends upon the time of diffusion which normally extends to 2 hours.
The diffusion of impurities normally takes place both laterally as well as vertically.
Therefore, the actual junction profiles will be curved as shown in Fig. 1.9. However, for the sake of simplicity, lateral diffusion will be omitted in all the drawings.



The cross-section of an *npn* transistor showing curved junction profiles as a result of lateral diffusion

4.3.7 ION IMPLANTATION

Ion implantation is the other technique used to introduce impurities into a silicon wafer. In this process, silicon wafers are placed in a vacuum chamber and are scanned by a beam of high-energy dopant ions (boron for p-type and phosphorus for n-type) as shown in Fig. 1.10. These ions are accelerated by energies between 20 kV to 250 kV. As the ions strike the silicon wafers, they penetrate some small distance into the wafer. The depth of penetration of any particular type of ion increases with increasing accelerating voltage. Ion implantation technique has two important advantages.

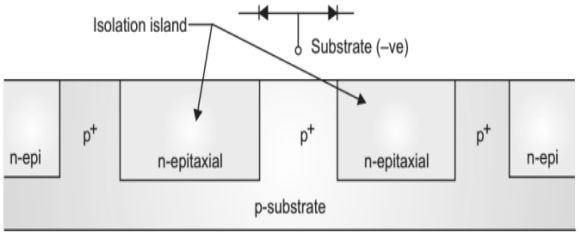
1) It is performed at low temperatures. Therefore, previously diffused regions have a lesser tendency for lateral spreading.
2) In diffusion process, temperature has to be controlled over a large area inside the oven, whereas in ion implantation technique, accelerating potential and the beam current are electrically controlled from outside.

4.3.8 ISOLATION

Since a number of components are fabricated on the same IC chip, it becomes necessary to provide electrical isolation between different components and interconnections. Various types of isolation techniques have been developed. However, we shall discuss here only two commonly used techniques

1) P-N JUNCTION ISOLATION

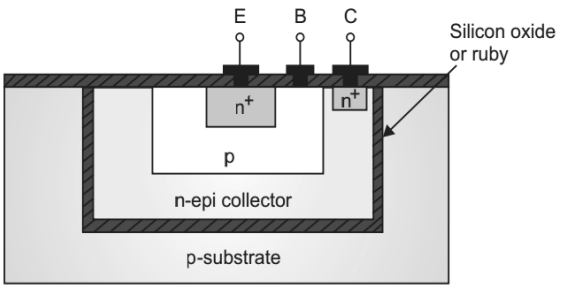
In this isolation technique, p+ type impurities are selectively diffused into the n-type epitaxial layer so as to reach p-type substrate as shown in Fig. 1.11 (a). This produces islands surrounded by p-type moats. It can be seen that these regions are separated by two back-to-back p-n junction diodes. If the p-type substrate material is held at the most negative potential in the circuit, the diodes will be reverse biased providing electric isolation between these islands. The different components are fabricated in these isolation islands. The concentration of the acceptor atoms in the region between isolation islands is usually kept much higher (p+) than the p-type substrate. This prevents the depletion region of the reverse biased diode from penetrating more into p+ region and possibly connecting the isolation islands.
There is, however, one undesirable by-product of this isolation process. It is the presence of a transition capacitance at the isolating pn junctions, resulting in an inevitable capacitor coupling between the components and the substrate. These parasitic capacitances limit the performance of the circuit at high frequencies. But being economical, this technique is commonly used for general purpose ICs.



p-n junction isolation

2) DIELECTRIC ISOLATION

Here a layer of solid dielectric such as silicon dioxide or ruby completely surrounds each component, thereby producing isolation, both electrical and physical. This isolating dielectric layer is thick enough so that its associated capacitance is negligible. Also, it is possible to fabricate both pep and nap transistor within the same silicon substrate. Since this method requires additional fabrication steps, it becomes more expensive. The technique is mostly used for fabricating professional grade ICs required for specialized applications via, aerospace and military, where higher cost is justified by superior performance. Figure 1.11 (b) shows such a structure.



Dielectric isolation

4.3.9 METALLIZATION

The purpose of this process is to produce a thin metal film layer that will serve to make interconnections of the various components on the chip. Aluminum is usually used for the metallization of most ICs as it offers several advantages.

1. It is relatively a good conductor.
2. It is easy to deposit aluminum films using vacuum deposition.
3. Aluminum makes good mechanical bonds with silicon.
4. Aluminum forms low resistance, non-rectifying (i.e., holmic) contact with p-type silicon and the heavily doped n-type silicon.

   The film thickness of about 1 mm and conduction width of about 2 to 25 mm are commonly used. The process takes place in a vacuum evaporation chamber as shown in Fig. 1.12. The pressure in the chamber is reduced to the range of about 10–6 to 10–7 torr (1 atmosphere = 760 torr = 760 mm Hg). The material to be evaporated is placed in a resistance heated tungsten coil or basket. A very high power density electron beam is focused at the surface of the material to be evaporated. This heats up the material to very high temperature and it starts vaporizing. These vapors travel in straight line paths. The evaporated molecules hit the substrate and condense there to form a thin film coating.

   After the thin film metallization is done, the film is patterned to produce the required interconnections and bonding pad configuration. This is done by photolithographic process and aluminum is etched away from unwanted places by using etchants like phosphoric acid (H_3PO_4).

4.3.10 ASSEMBLY PROCESSING & PACKAGING

Each of the wafer processed contains several hundred chips, each being a complete circuit. So, these chips must be separated and individually packaged. A common method called scribing and cleaving used for separation makes use of a diamond tipped tool to cut lines into the surface of the wafer along the rectangular grid separating the individual chips. Then the wafer is fractured along the scribe lines and the individual chips are physically separated. Each chip is then mounted on a ceramic wafer and attached to a suitable package. There are three different package configurations available:

1) Metal can package
2) Ceramic flat package
3) Dual-in-line (ceramic or plastic type) package.

4.4 FABRICATION OF A TYPICAL CIRCUIT

We shall here show the various steps utilized in converting the circuit into monolithic IC

STEP-1 WAFER PREPARATION

Refer Fig. (a). The starting material called the substrate is a p-type silicon wafer prepared as discussed in Sec. 1.5.1. The wafers are usually of 10-cm diameter and 0.4 mm (~ 400 μ m) thickness. The resistivity is approximately 10 W-cm corresponding to concentration of acceptor atom, $N_A = 1.4 \times 10^{15}$ atoms/cm^3.

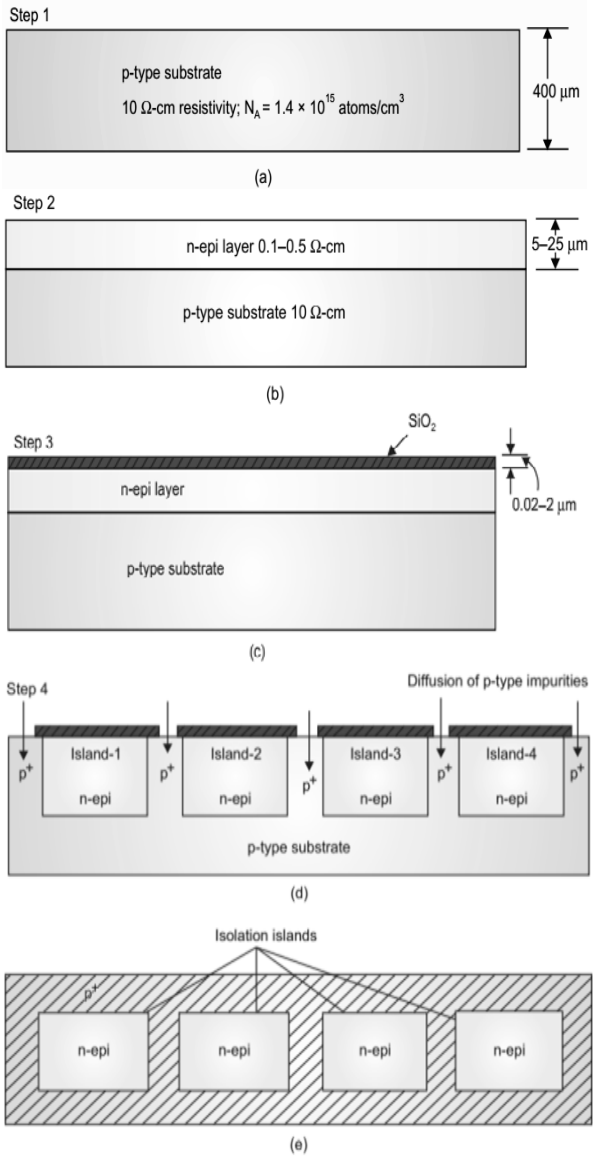
STEP-2 EPITAXIAL GROWTH

An n-type epitaxial film (5–25 μm) is grown on the p-type substrate as shown in Fig. (b). This ultimately becomes the collector region of the transistor, or an element of the diode a nd diffused capacitor associated with the circuit. So, in

general it can be said that all active and passive components are fabricated within this layer. The resistivity of n-epitaxial layer is of the order of 0.1 to 0.5Ω − cm.

STEP-3 OXIDATION

Refer Fig. (c). A SiO2 layer of thickness of the order of 0.02 to 2 μm is grown on theN-epitaxial layer.

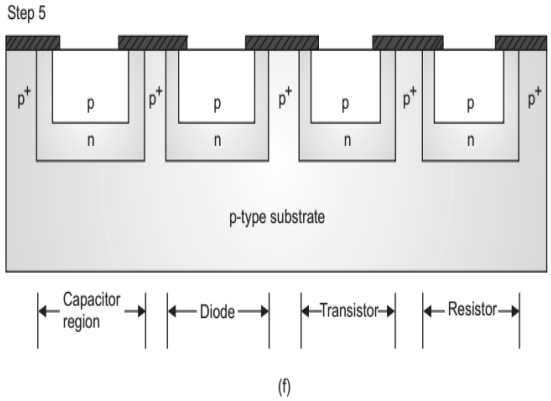


STEP-4 ISOLATION DIFFUSION

If in the circuit four components have to be fabricated, so we require four islands which are isolated. For this, SiO2 is removed from five different places using photolithographic technique. Refer Fig. (d). The wafer is next subjected to heavy p-type diffusion for a long time interval so that p-type impurities penetrate the n-type epitaxial layer and reach the p-type substrate. The areas under the SiO2 are n-type islands that are completely surrounded by p-type moats. As long as the pn junctions between the isolation islands are held at reverse bias, that is, the p-type substrate is held at a negative potential with respect to the n-type isolation islands, these regions are electrically isolated from each other by two back-to-back diodes, providing the desired isolation. The concentration of acceptor atoms ($N_A \cong 5 \times 10^{20} cm^{-3}$) in the region between isolation islands is generally kept higher than p-type substrate for which$N_A = 1.4 \times 10^{15} atoms/cm^3$. This ensures that the depletion region of the reverse biased diode will not extend into p+ region to the extent of electrically connecting the two isolation islands. There will, however, be a significant amount of barrier or transition capacitance present as a byproduct of the isolation diffusion. The top view of the isolation islands is depicted in Fig. (e).

STEP-5 BASE DIFFUSION

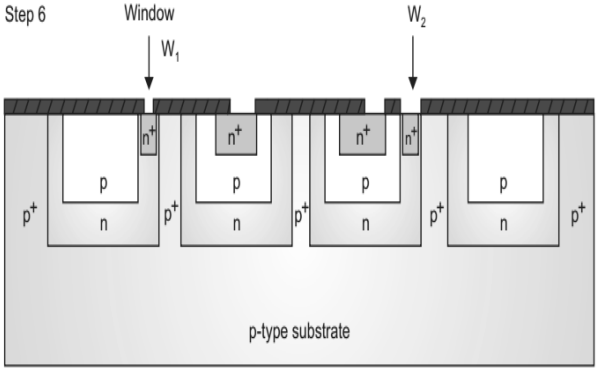
Refer to Fig. (f). A new layer of SiO_2 is grown over the entire wafer and a new pattern of openings is formed using photolithographic technique. Now, p-type impurities, such as boron, are diffused through the openings into the islands of n-type epitaxial silicon. The depth of this diffusion must be controlled so that it does not penetrate through n-layer into the substrate. This diffusion is utilized to form base region, of the transistor, resistor, and the anode of the diode and junction capacitor.



STEP-6 EMITTER DIFFUSION

Refer to Fig. (g) A new layer of SiO_2 is again grown over the entire wafer and selectively etched to open a new set of windows and n-type impurity (phosphorus) is diffused through them. This forms transistor emitter and cathode region of diode. Windows (W1, W2 etc.) are also etched into n-region where contact is to be made to the n-type layer. Heavy concentration of phosphorus (n^+) is diffused into these regions simultaneously with the emitter diffusion. The reason for using heavily-doped n-regions can be explained as follows:

Aluminum, normally used for making interconnections, is a p-type impurity in silicon, and can produce an unwanted rectifying contact with the lightly-doped n-material. However, heavy concentration of phosphorous ($\sim 2 \times 10^{20} cm^{-3}$) doping causes a high degree of damage to the Si-lattice at the surface, thus effectively making it semi-metallic. This n+ layer thus makes a good ohmic contact with the Al-layer.



(g)

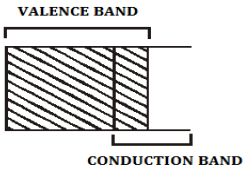
ASSIGNMENT QUESTIONS

Q.1 At room temperature, the current in an intrinsic semiconductor is due to
a) Holes b) Electrons
c) Ions d) Holes and electrons

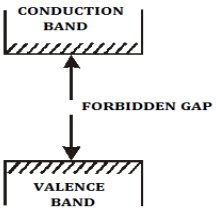
Q.2 Match List I with List II and select the correct answer using the codes given below the lists:

List I (List of materials)
A) Conductor
B) Semiconductor
C) Insulator

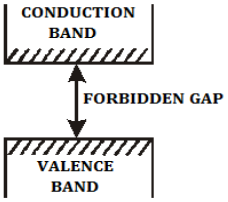
List II (Energy-band diagram)
1)



2)



3)



Codes:

	A	B	C
a)	1	3	2
b)	3	1	2
c)	1	2	3
d)	2	3	1

Q.3 For a photoconductor with equal electron and hole mobilities and perfect ohmic contacts at the ends, an increase in the intensity of optical illumination results in
a) A change in open circuit voltage
b) A change in short-circuit current
c) A reduction of resistance
d) An increase of resistance

Q.4 A sample of N-type semiconductor has electron density of $6.25 \times 10^{18}/cm^3$ at 300 K. If the intrinsic concentration of carriers in this sample is $2.5 \times 10^{13}/cm^3$, at this temperature, the hole density works out to be
a) $10^6/cm^3$ b) $10^8/cm^3$
c) $10^{10}/cm^3$ d) $10^{12}/cm^3$

Q.5 If the drift velocity of holes under a field gradient of 100 V/m is 5m/s their mobility (in the same SI units) is
a) 0.05 b) 0.5
c) 50 d) 500

Q.6 Which of the following statements relate to the Hall effect?
1. A potential difference is developed across a current-carrying metal strip when the strip is placed in a transverse magnetic field.
2. The Hall effect is very weak in metals but is large in semiconductors.
3. The Hall effect is very weak in semiconductors but is large in metals.
4. It is applied in the measurement of the magnetic field intensity.

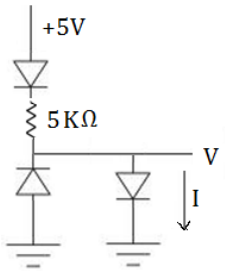
Select the correct answer using the codes given below:
a) 1, 2 and 3 b) 2 and 4
c) 1, 3 and 4 d) 1, 2 and 4

Q.7 The conductivity of a semiconductor crystal due to any current carrier is NOT proportional to
a) Mobility of the carrier
b) Effective density of states in the conduction Band
c) Electronic charge
d) Surface states in the semiconductor

Q.8 Consider a semiconductor bar having square cross-section. Assume that holes drift in the positive x-direction and a magnetic field is applied perpendicular to the direction in which holes drift(+ve z direction) . The sample will show
a) A negative resistance in positive y-direction.
b) A positive voltage in positive y direction
c) A negative voltage in positive y-direction
d) A magnetic field in positive y-direction.

Q.9 A resistance thermometer has a temperature coefficient of resistance 10^{-3} per degree and its resistance at $0^{o}C$ is 1.0Ω. At what temperature is its resistance 1.1Ω ?
a) $10^{o}C$ b) $100^{o}C$
c) $120^{o}C$ d) $-10^{o}C$

Q.10 Calculate V and I assume diode drop of 0.7V.



a) 1.4 V & 720μA b) 1.4 V &720mA
c) 0.7 V & 720μA d) 0.7 V & 720mA

Q.11 A semiconductor specimen of breadth d, width w and carrying current I is placed in a magnetic field B to develop Hall voltage V_H in a direction perpendicular to I and B. V_H is NOT proportional to
a) B b) I
c) 1/w d) 1/d

Q.12 In switching diode fabrication, a dopant is introduced into silicon which introduces additional trap levels in the material thereby reducing the mean life time of carriers. This dopant is:
a) Aluminum b) Platinum
c) Gold d) Copper

Q.13 Match List I (Equation) with List II (Relation between/Description) and select the correct answer using the codes given below the lists:

List I (Equation)
a) Continuity
b) Einstein's equation
c) Poisson's equation
d) Diffusion equation

List II (Relation between /Description)
1) Relates diffusion constant with mobility.
2) Relates charge density with electric field
3) Relates flow with rate of change of Concentration in space
4) Rate of change of minority carrier Density with time

Codes:

	A	B	C	D
a)	4	1	3	2
b)	4	1	2	3
c)	1	4	2	3
d)	1	4	3	2

Q.14 Match List I (Material) with List II (Band Gap) and select the correct answer using the codes given below the lists:

List I (Material)
a) Metal
b) Semimetal

c) Semiconductor
d) Insulator

List II (Band Gap)

1) 9 eV
2) 0.05 eV
3) 1.5 eV
4) 0 or less

Codes:

	A	B	C	D
a)	4	2	3	1
b)	4	3	2	1
c)	1	3	2	4
d)	1	2	3	4

Q.15 A copper wire is 1 meter long and has a uniform cross-section of 0.1 mm^2. The resistance of the wire at room temperature is 0.171 ohm. What is the resistivity of the material?

a) $1.71\times10^{-6}\Omega m$ b) $1.71\times10^{-7}\Omega m$

c) $1.71\times10^{-8}\Omega m$

d) $1.71\times10^{-9}\Omega m$

Q.16 What is the approximate mobility of holes in Germanium at room temperature?

a) 4500 $cm^2/V.s$ b) 2400 $cm^2/V.s$
c) 1800 $cm^2/V.s$ d) 900 $cm^2/V.s$

Q.17 The mobility of electrons in a semiconductor is defined as the

a) Diffusion velocity per unit electric field.
b) Diffusion velocity per unit magnetic field.
c) Drift velocity per unit magnetic field
d) Drift velocity per unit electric field

Q.18 The free electron density in a conductor is $(1/1.6)\times10^{22}$ cm^{-3}. The electron mobility is 10 cm^2/V s. What is the value of its resistivity?

a) 10^{-4}Wm b) 1.6' 10^2Wm
c) $10^{-4}\Omega$ cm d) 10^4 mho cm^{-1}

Q.19 The intrinsic concentration in a semiconductor at 300 K is 10^{13} cm^{-3}. When it is doped with donor type impurities, the majority carrier concentration becomes 10^{17} cm^{-3}. What is the value of its minority carrier density?

a) 0.999' 10^{17} cm^{-3} b) 10^{17} cm^{-3}
c) 10^4 cm^{-3} d) 10^9 cm^{-3}

Q.20 Which one of the following is the correct relationship between the band gap of a material used in a photo detector and the energy of the incident photon? (the symbols have usual meanings)

a) $E_g \geq hc/\lambda$ b) $hv^2/l^3 \leq E_g$

c) $hv \geq E_g$ d) $\frac{1}{2}hv \leq E_g$

Q.21 Two pure specimen of a semiconductor material are taken. One is doped with 10^{18} cm^{-3}number of donors and the other is doped with 10^{16} cm^{-3}number of acceptors. The minority carrier density in the first specimen is10^7 cm^{-3}. What is the minority carrier density in the other specimen ?

a) $10^{16}cm^{-3}$ b) 10^{27} cm^{-3}
c) $10^{18}cm^{-3}$ d) 10^9 cm^{-3}

Q.22 Match List I (Type of Conductor) with List II (Position of Fermi Level) and select the correct answer using the code given below the lists:

List I (Type of Conductor)

a) n-type semiconductor
b) p-type semiconductor
c) Intrinsic semiconductor
d) Degenerate n-type S.C

List II (Position of Fermi Level)

1)Middle of band gap
2)Above conduction band
3)Near but below conduction band
4)Near but above valance band.

Code: **A** **B** **C** **D**

a)	1	2	3	4
b)	3	4	1	2
c)	1	4	3	2
d)	3	2	1	4

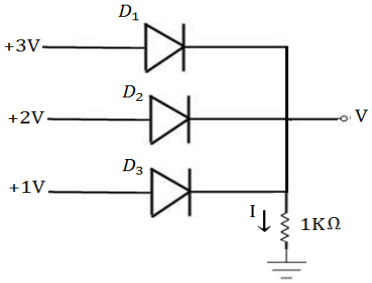
Q.23 Diffusion of impurities in a semiconductor is carried out in a furnace through which a steady stream of impurity atoms is passed during the entire diffusion process. What would be the type of profile of the impurity atoms inside the semiconductor?
a) Linear
b) Gaussian
c)Complementary error function
d) Exponential

Q.24) Which one of the following statements is correct in respect of the use of Direct Gap (DG) and Indirect Gap (IG) semiconductors in fabrication of Light Emitting Diode?
a) Both DG and IG semiconductors are suitable.
b) Only DG semiconductor is suitable.
c) DG semiconductor is suitable and some IG materials having proper dopants are also used.
d) Only IG semiconductors are suitable.

Q.25 The basic function of buried n^+ layer in an n-p-n transistor fabricated in IC is to
a) Reduce the magnitude of the base spreading resistance.
b) Reduce the collector series resistance
c) Reduce the base width of the transistor
d) Increase the gain of the transistor.

Q.26 The wavelength of light emitted by a GaAs laser is 8670×10^{-10} m. Given Plank's constant = 6.626×10^{-34}Js, velocity of light = 2.998×10^{8} ms^{-1} and 1 eV = 1.602×10^{-19} J, the energy gap in GaAs is
a) 0.18eV b) 0.7eV
c) 1.43eV d) 2.39 eV

Q.27 Calculate V and I. Assume voltage drop across the diode of 0.7 V



a) 2.3 V & 2.3mA b) 1 V & 1mA
c) 2 V & 2mA d) 3 V & 3mA

Q.28 Match List I (Crystal type) with List II (Name of the solid) and select the correct answer using the codes given below the lists:
List I
a) Ionic
b) Covalent
c) Metallic
d) Van der Wall's
List II
1) Solid argon
2) Copper
3) Silicon
4) Sodium chloride
Codes:

	A	**B**	**C**	**D**
a)	3	4	2	1
b)	4	3	1	2
c)	3	4	1	2
d)	4	3	2	1

Q.29 The carrier mobility in a semiconductor is $0.4 m^2/Vs$. Its diffusion constant at 300 K will be (in m^2/s)
a) 0.43 b) 0.16
c) 0.04 d) 0.01

Q.30 Silicon diode is less suited for low voltage rectifier operation because

a) It can withstand high temperatures
b) Its reverse saturation current is low
c) Its cut-in voltage is high
d) Its breakdown voltage is high

Q.31 Gold is often diffused into silicon PN junction devices to
a) Increase the recombination rate
b) Reduce the recombination rate
c) Makes silicon a direct gap semiconductor
d) Make silicon semi-metal

Q.32 Silicon is not suitable for fabrication of light emitting diodes because it is
a) An indirect band gap semiconductor
b) A direct band gap semiconductor
c) A wide band gap semiconductor
d) A narrow band gap semiconductor

Q.33 The change in barrier potential of a silicon p-n junction with temperature is
a) 0.025 Volts per degree C
b) 0.250 Volts per degree C
c) 0.030 Volts per degree C
d) 0.014 Volts per degree C

Q.34 The diffusion capacitance of a p-n junction diode
a) Increases exponentially with forward bias voltage.
b) Decreases exponentially with forward bias voltage
c) Decreases linearly with forward bias voltage.
d) Increase linearly with forward bias voltage.

Q.35 The reverse current of a silicon diode is :
a) Highly bias voltage sensitive.
b) Highly temperature sensitive
c) Both bias voltage and temperature sensitive.
d) Independent of bias voltage and temperature.

Q.36 A combination of two diodes connected in parallel when compared to a single diode can withstand
a) Twice the value of peak inverse voltage.
b) Twice the value of maximum forward current
c) A larger leakage current
d) Twice the value of cut-in voltage.

Q.37 The light emitting diode (LED) emits light of a particular color because
a) It is fabricated from a fluorescent material.
b) Transition between energy levels of the carriers takes place while crossing the p-n junction
c) Heat generated in the diode is converted into light.
d) The band gap of the semi-conductor material used in the fabrication of the diode is equal to the energy $\frac{hc}{\lambda}$ of the light photon.

Q.38 Depletion capacitance in a diode depends on:
1. Applied Junction voltage.
2. Junction built-in potential.
3. Current through junction
4. Doping profile across the junction
Select the correct answer using the codes given below:
a) 1 and 2 b) 1 and 3
c) 1, 2 and 4 d) 2, 3 and 4

Q.39 The depletion region in a semiconductor p-n junction diode has
a) Electrons and holes
b) Positive and negative ions on either side
c) Neither electrons nor ions
d) No holes

Q.40 When a junction diode is used in switching applications, the forward recovery time is:
a) Of the order of the reverse recovery time.
b) Negligible in comparison to the reverse recovery time.
c) Greater than the reverse recovery time.
d) Equal to the mean carrier life time τ for the excess minority carriers.

Q.41 Match **List I (Diode)** with **List II (Application)** and select the correct answer using the codes given below the lists:

List I (Diode)
a) Varactor diode
b) Tunnel diode
c) Photodiode
d) Zener diode

List II (Application)
1) To charge auxiliary storage batteries
2) Reference voltage
3) High frequency tuning circuits
4) High frequency switching circuit.

Codes:

	A	B	C	D
a)	2	1	4	3
b)	3	1	4	2
c)	3	4	1	2
d)	2	4	1	3

Q.42 The junction capacitance of a p-n junction depends on
a) Doping concentration only
b) Applied voltage only
c) Both doping concentration and applied voltage.
d) Barrier potential only

Q.43 In a p-n junction, the space charge capacitance is proportional to V^{-n} where V is the applied bias voltage and 'n' is a constant. The value of 'n' for step, linearly graded and diffused junctions would be respectively.
a) $\frac{1}{2}\frac{1}{3}\frac{1}{2.5}$ b) $\frac{1}{3}\frac{1}{2}\frac{1}{2.5}$
c) $\frac{1}{2}\frac{1}{2.5}\frac{1}{3}$ d) $\frac{1}{3}\frac{1}{2.5}\frac{1}{2}$

Q.44 A p-n junction diode's dynamic conductance is directly proportional to
a) the applied voltage
b) the temperature
c) its current
d) the thermal voltage

Q.45 When a junction transistor is operated under saturated conditions
a) Both the CB and EB junctions are forward biased.
b) The CB junction is forward biased but the EB junction is reverse biased.
c) The CB junction is reverse biased but the EB junction is forward biased.
d) Both the CB junction are reverse biased.

Q.46) The collector to emitter cut-off current (I_{CEO}) of a transistor is related to collector to base cut-off current (I_{CBO}) as (α is the CB current gain of the transistor)
a) $I_{CEO} = I_{CBO}$ b) $I_{CEO} = \alpha I_{CBO}$
c) $I_{CEO} = \frac{I_{CBO}}{1-\alpha}$ d) $I_{ECO} = \frac{I_{CBO}}{1+\alpha}$

Q.47 A bipolar junction transistor has a common base forward short circuit current gain of 0.99. Its common emitter forward short circuit current gain will be
a) 50 b) 99
c) 100 d) 200

Q.48 A bipolar junction transistor is in saturation region. Given V_{CC} = 10V,

$R_C = 1k\Omega$, $h_{FE} = 100$ and $V_{CE\,sat} = 0.3$ V. What is the collector current in saturation?

a) 10 mA b) 9.7 mA
c) 0 mA d) 1 mA

Q.49 Match List I (Regions of bipolar transistor in a monolithic IC) with List II (Physical properties) and select the correct answer using the codes given below the lists:

List I

A. Emitter
B. Base
C. Collector
D. Substrate

List II

1. Moderate resistivity
2. Very high resistivity
3. Large size
4. Very high conductivity

Codes:

	A	B	C	D
a)	1	4	2	3
b)	4	1	2	3
c)	4	1	3	2
d)	1	4	3	2

Q.50 If $\alpha = 0.995$, $I_E = 10$mA and $I_{co} = 0.5\mu$A, then I_{CEO} will be

a) 100μA b) 25μA
c) 10.1 mA d) 10.5mA

Q.51 In a transistor amplifier, the reverse saturation current I_{CO}

a) Doubles for every 10°C rise in temperature.
b) Doubles for every 1°C rise in temperature.
c) Increase linearly with temperature
d) Doubles for every 5°C rise in temperature.

Q.52 A transistor emitter base voltage (V_{EB}) of 20 mV has a collector current (I_C) of 5 mA. For V_{EB} of 30 mV, I_C is 30 mA. If V_{EB} is 40 mV, then the I_C will be

a) 55mA b) 160 mA
c) 180 mA d) 270 mA

Q.53 In a junction transistor, the collector cut-off current 'I_{CBO}' reduce considerably by doping the

a) Emitter with high level of impurity
b) Emitter with low level of impurity
c) Collector with high level of impurity
d) Collector with low level of impurity

Q.54 Thermal runaway will take place if the quiescent point is such that

a) $V_{CE} > \frac{1}{2}V_{CC}$ b) $V_{CE} < V_{CC}$

c) $V_{CE} < 2V_{CC}$ d) $V_{CE} < \frac{1}{2}V_{CC}$

Q.55 The drain source output V-I characteristics of an n-channel depletion FET has

a) $I_{DS} = 0$ at $V_{GS} = 0$
b) I_{DS} = positive maximum at $V_{GS} = 0$
c) I_{DS} = negative maximum at $V_{GS} = 0$
d) I_{DS} = independent of V_{GS}

Q.56 The output V-I characteristics of an enhancement type MOSFET has

a) Only an ohmic region
b) Only a saturation region
c) An ohmic region at low voltage value followed by a saturation region at higher voltage.
d) An ohmic region at large voltage values preceded by a saturation region at lower voltages.

Q.57 For an n-channel JFET, having drain-source voltage constant if the gate source voltage is increased (more negative) pinch-off would occur for

a) High values of drain current
b) Saturation value of drain current
c) Zero drain current
d) Gate current equal to the drain current

Q.58 In modern MOSFETs, the material used for the gate is
a) High purity silicon
b) High purity silica
c) Heavily doped polycrystalline silicon
d) Epitaxial grown silicon

Q.59 A FET a better chopper than a BJT because it has
a) Lower off-set voltage
b) Higher series ON resistance
c) Lower input current
d) Higher input impedance

Q.60 The output current versus input voltage transfer characteristic of an n-channel JFET is such that there is
a) Zero current flow at zero input voltage bias
b) Current flow only when a positive input threshold voltage is crossed.
c) Current flow only when a negative input cut-off voltage bias is crossed.
d) No cut-off input voltage

Q.61 In an MOS transistor, the gate source input impedance is
1. Lower than the input impedance of a BJT
2. Higher than the input impedance of a BJT
3. Lower than the input impedance of a JFET
4. Higher than the input impedance of a JFET

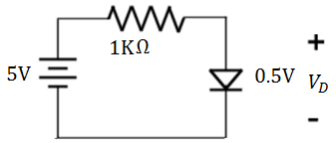
Select the correct answer using the codes given below:

Codes:

a) 1 alone b) 2 and 3
c) 4 alone d) 2 and 4

Q.62 Thermal runaway is not possible in FET because as the temperature of FET increases
a) the mobility decreases
b) thetransconductance increases
c) the drain current increases
d) the mobility increases.

Q.63 The diode has threshold voltage of 0.5 V and forward resistance of 1Ω. The current I and voltage drop V_d across diode are.



a) 5mA & 0.5V
b) 5mA & 5V
c) 4.469mA & 0.5 V
d) 4.496mA & 5V

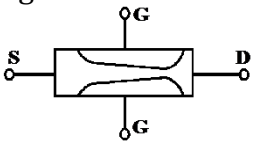
Q.64 The voltage gain of a given common source JEFT amplifier depends on its
a) Input impedance
b) Amplification factor
c) Dynamic drain resistance
d) Drain load resistance

Q.65 The threshold voltage of an n-channel enhancement mode MOSFET is 0.5V. When the device is biased at a gate voltage of 3V. Pinch off would occur at a drain voltage of
a) 1.5V b) 2.5V
c) 3.5V d) 4.5V

Q.66 Consider the following devices:
1. BJT in CB mode.
2. BJT in CE mode
3. JEFT`
4. MOSFET

The correct sequence of these devices in increasing order of their input impedances is:
a) 1,2,3,4 b) 2,1,3,4
c) 2,1,4,3 d) 1,3,2,4

Q.67 In a biased JFET, the shape of the channel is as shown in the given figure because



a) It is the property of the material used
b) The drain end is more reverse biased than source end
c) The drain end is more forward biased than source end
d) The impurity profile varies with the distance from source.

Q.68 What is the correct sequence of the following step in the fabrication of a monolithic, bipolar junction transistor?
1. Emitter diffusion
2. Base diffusion
3. Buried layer formation
4. Epi-layer formation
Select the correct answer using the codes given below:
a) 3, 4, 1, 2 b) 4, 3, 1, 2
c) 3, 4, 2, 1 d) 4, 3, 2, 1

Q.69 In an integrated circuit, the SiO_2 layer provides
a) Electrical connection to external circuit
b) Physical length
c) Isolation
d) Conducting path

Q.70 As the Fermi energy of silver is 8.8×10^{-19} joule, the velocity of the fastest electron in silver at 0K (Given : Rest mass of electron = 9.1×10^{-31}kg.)is
a) 3.33×10^{5}m/s b) 4.40×10^{7}m/s
c) $1.39\times10^{6} m/s$ d) $3\times10^{8} m/s$

Q.71 Electron mobility and life-time in a semiconductor at room temperature are respectively $0.36m^2/(Vs)$ and 340 μs. The diffusion length is
a) 3.13 mm b) 1.77 mm
c) 3.55 mm d) 3.13 cm

Q.72 When a semiconductor bar is heated at one end, a voltage across the bar is developed. If the heated end is positive, the semiconductor is
a) p-type b) n-type
c) Intrinsic d)Highly degenerate

Q.73 Why does the mobility of electrons in a semiconductor decrease with increasing donor density?
a) Doping increases the effective mass of electrons
b) Doping decreases the relaxation time of electrons
c) Electrons are trapped by the donors
d) More holes are generated so that the effective mobility decreases

Q.74 An intrinsic semiconductor with energy gap 1 eV has a carrier concentration N at temperature 200 K. Another intrinsic semiconductor has the same value of carrier concentration N at temperature 600 K. What is the energy gap value for the second semiconductor?
a) (1/3) eV b) (3/2) eV
c) 3 eV d) 9 eV

Q.75 An intrinsic semiconductor is doped lightly with P – type impurity. It is found that the conductivity actually decreases till a certain doping level is reached. Why does the occur?
a) The mobility of holes decreases
b) The mobility of both electrons and holes decreases
c) The hole density actually reduces
d) Effect of reduction in electrons due to increase in holes compensates more than the effect of increase in holes on conductivity

Q.76 Consider the following statements with regard to semiconductors:
1. In n type material free electron concentration is nearly equal to density of donor atoms.

2. 1 part in 10^8 donor type impurity added to Ge improves its conductivity at 30°C by a factor 12.
3. Phosphorus is an example of n type impurity.

Which of these statements are correct?

a) 1, 2 and 3 b) 1 and 3 onl
c) 2 and 3 only d) 1 and 2 only

Q.77 In which one of the following ways can the Hall voltage across an impurity semiconductor crystal be increased?

a) By increasing the thickness of the crystal
b) By increasing the concentration of impurity atoms in the crystal
c) By increasing the width of the crystal
d) By increasing the current flowing through the crystal

Q.78 The Fermi function for an electron is f(E),where E is energy. Then, the Fermi function for a hole is

a) f(E) b) 1 –f(E)
c) 1/f(E) d) 1 + f(E)

Q.79 The initial temperature of a specimen of silicon is $T_1 = 300K$. By what factor does the intrinsic concentration n_i increase if the temperature increase by 10 °C (18°F)? Assume the band gap at both temperatures is $E_G = 1.11eV$.

a) 3 b) 1/3
c) 1/2 d) 2

Q.80 Consider the following statements for an n-type semiconductor:

1. E_F lies below E_D at a room temperature (T)
2. E_F lies above E_D as $T \rightarrow 0$
3. E_F = E_D at some intermediate temperature.
4. E_F is invariant with temperature.

Where $E_F$is Fermi energy and E_D is donor level energy.

Which of these statements is/are correct

a) 1 and 2 b) 2 and 3
c) 4 only d) 1, 2 and 3

Q.81 Consider the following statements:

A semiconductor to be used in optoelectronic devices should have

1. Direct energy band gap.
2. Indirect energy band gap.
3. Any value of forbidden energy band gap.
4. Right value of band gap corresponding to light wavelength.

Which of the statement is /are correct?

a) 1 only b) 1 and 4
c) 2 and 3 d) 2 and 4

Q.82 Which one of the following is the correct statement?

The type of majority charge carriers in a semiconductor can be found by

a) Hall effect
b) Piezoelectric effect
c) Photoelectric effect
d) Meissner effect

Q.83 Assuming the Fermi level E_F to be independent of temperature, E_F may be defined as the level with an electron occupancy probability of

a) 0% b) 50%
c) 75% d) 100%

Q.84 Which of the following has the greatest mobility?

a) Positive ion b) Negative ion
c) Electron d) Hole

Q.85 An intrinsic semiconductor at a temperature of absolute zero behaves like an insulator because of

a) Non-availability of free electrons
b) Non-recombination of electrons with holes
c) Low drift velocity of free electrons

d) Low (almost zero) electron energy

Q.86 With an increase in temperature, the Fermi level in an intrinsic semiconductor
a) Moves closer to the conduction band edge
b) Moves closer to the valence band edge
c) Moves into the conduction ban
d) Remains at the centre of the forbidden gap

Q.87 On which of the following factors does the electrical conductivity of a semiconductor depend?
1. Carrier concentration
2. Carrier mobility
3. Sign of the carrier
Select the correct answer using the codes given below:
a) 1 and 2 b) 1 and 3
c) 2 and 3 d) 1, 2 and 3

Q.88 An LED made using GaAs emits radiation in:
a) Visible region
b) Ultraviolet region
c) Infra red region
d) Microwave frequency region.

Q.89 **Assertion (A):** An unbiased p-n junction develops a built-in potential at the junction with the n-side positive and the p-side negative.
Reason (R): The p-n junction behaves as a battery and supplies current to a resistance connected across its terminals.
a) Both A and R are individually true and R is the correct explanation of A
b) Both A and R are individually true but R is not the correct explanation of A
c) A is true but R is false
d) A is false but R is true

Q.90 A MOs capacitor has $t_{ox} = 5nm$.If the maximum depletion layer width is 61nm, the minimum capacitance is.
$(\in_{SiO_2} = 3.9 \in_0)(\in_{Si} = 12 \in_0)$
a) $1.74 \frac{mF}{m^2}$ b) $2 \frac{mF}{m^2}$
c) $1.39 \frac{mF}{m^2}$ d) $6.9 \frac{mF}{m^2}$

Q.91 In a forward biased photo diode, an increase in incident light intensity causes the diode current to
a) Increase
b) Remain constant
c) Decrease
d) Remain constant while the voltage drop across the diode increases

Q.92 The junction capacitance of a linearly graded junction varies with the applied reverse bias V_r as
a) V_r^{-1} b) $V_r^{-\frac{1}{2}}$
c) $V_r^{-\frac{1}{3}}$ d) $V_r^{\frac{1}{2}}$

Q.93 A PN junction in series with a 100 ohm resistor is forward biased so that a current of 100mA flows. If voltage across the combination is instantaneously reversed to 10V at time t= 0, the reverse current that flows through the junction at t = 0 is approximately given by
a) 0 mA b) 200 mA
c) 50 mA d) 100 mA

Q.94 The development of barrier potential in the depletion zone of a PN junction is consequent to
a) Diffusion of majority carriers across junction
b) Drift of minority carriers across junction
c) Generation of minority carriers due to thermal energy

d) Initial flow of conduction current

Q.95 The current flowing in a certain PN junction at room temperature 300 K is 2×10^{-7} A when a large reverse bias voltage is applied. The current flowing when a forward bias of 0.1 V is applied will be

a) $2\times10^{-7}\exp\left[\frac{-1.6\times10^{-19}\times0.1}{1.38\times10^{-23}\times300}\right]$

b) $2\times10^{-7}\left[\frac{1.6\times10^{-19}\times0.1}{1.38\times10^{-23}\times300}\right]$

c) $2\times10^{-7}\exp\left[\frac{-1.38\times10^{-23}\times300}{1.6\times10^{-19}\times0.1}\right]$

d) $2\times10^{-7}\left[\frac{1.38\times10^{-23}\times300}{1.6\times10^{-19}\times0.1}\right]$

Q.96 Which of the following main properties of a bipolar junction transistor, make it necessary for the transistor to have bias stabilization?

1. Variation of V_{BE} with temperature
2. Variation of h_{FE} with temperature
3. Variation of I_{CO} with temperature
4. Variation of h_{FE} with transistor replacement
5. Variation V_{BE} with transistor replacement
6. Variation of I_{CO} with transistor replacement.

Select the correct answer using the codes given below:

a) 1, 2 and 6 b) 1, 3 and 4
c) 2, 3 and 5 d) 3, 4, 5 and 6

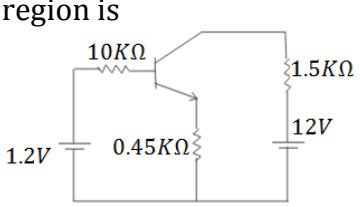
Q.97 The p-type epitaxial layer grown over an n-type substrate for fabricating a bipolar transistor will function as

a) The collector of a p-n-p transistor
b) The base of an n-p-n transistor
c) The emitter of a p-n-p transisto
d) The collector contact for a p-n-p transistor

Q.98 The conductivity of the intrinsic germanium at 300°K when, n_i at 300°K = 2.5 X 10^{13}/cm and μ_n and μ_p in germanium are 3800 and 1800 cm^2/Vs respectively.

a) 0.224 S/cm b) 0.0224 S/cm
c) 2.24 S/cm d) 0.00224 S/cm

Q.99 For the circuit shown in the above figure, by assuming β=200 and V_{BE} =0.7 V, the best approximation for the collector current I_c in the active region is



a) 1 mA b) 2.4 mA
c) 3 mA d) 9.6 mA

Q.100 Early effect in BJT refers to

a) Avalanche breakdown
b) Thermal runway
c) Base narrowing
d) Zener breakdown

Q.101 Almost all resistors are made in a monolithic integrated circuit

a) During the emitter diffusion
b) While growing the epitaxial layer
c) During the base diffusion
d) During the collector diffusion

Q.102 The main disadvantage of JFET is

a) Low gain bandwidth product
b) High noise level
c) High cost
d) Low gain

Q.103 The current amplification factor β can never be

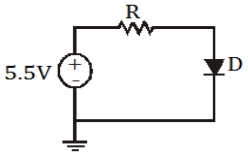
a) = 100 b) > 1
c) < 1 d) none of these

Q.104 In a common base transistor circuit, the current gain is 0.98. On changing emitter current by 5.00 mA, the change in collector current is:

a) 0.196 mA b) 2.45 mA
c) 4.90 mA d) 5.10 mA

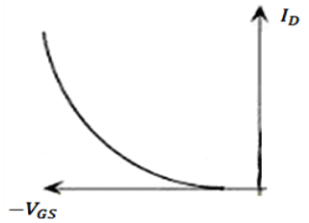
Q.105 In a P-N junction having depletion layer of thickness 10^{-6} m, the potential across it is 0.1V. The electric field is
a) 10^{7} V/m b) 10^{-6} V/m
c) 10^{5} V/m d) 10^{-5} V/m

Q.106 The cut-in voltage V_T and the thermal voltage V_T for the diode D in fig. are 0.498 V and 2 mV, respectively. If the value of resistor R is 20Ω, the current flowing through the diode is



a) 275mA b) 250mA
c) 200mA d) less than 200mA

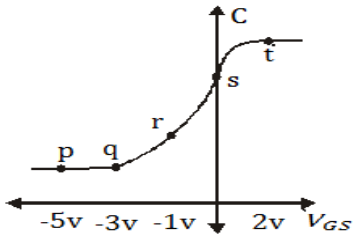
Q.107 TheI_D $-V_{GS}$ characteristics shown in fig is of



a) an enhancement type P MOSFET
b) an enhancement type N MOSFET
c) a depletion type PMOSFET
d) a depletion type NMOSFET

Q.108 A magnetic field $\overline{B}$ of 2 T is normal to a copper strip 0.5 mm thick carrying an electron current of 40 A. If the electron density is 10.0×10^{28} per cubic metre, then voltage across the strip in micro volt is
a) 40 b) 30
c) 20 d) 10

Q.109 The high-frequency C-V_{GS} characteristic of a MOSFET is shown in fig. In the curve, the accumulation condition is shown by the point



a) p b) q
c) s d) t

Q.110 The diffusion constant and mobility for electrons in a semiconductor material at a given temperature are 20 cm^2/s and 1600 $cm^2/V\text{-}s$, respectively. The thermal voltage V_T for a diode made of this material at the same temperature is
a) 125 mV b) 32 mV
c) 12.5 mV d) 3.2 mV

Q.111 In a P – well fabrication process, the substrate is
a) N-type semiconductor and is used to build P-channel MOSFET
b) P-type semiconductor and is used to build P-channel MOSFET
c) N-type semiconductor and is used to build N-channel MOSFET
d) P-type semiconductor and is used to build N-channel NOSFET

Q.112 At a given temperature, a semiconductor with intrinsic carrier concentration $n_i = 10^{16}/m^3$ is doped with a donor dopant of concentration $N_D = 10^{26}/m^3$. Temperature remaining the same, the hole concentration in the doped semiconductor is
a) $10^{26}/m^3$ b) $10^{16}/m^3$
c) $10^{14}/m^3$ d) $10^{6}/m^3$

Q.113 In a MOS capacitor with n-type silicon substrate, the Fermi potential Φ_F = - 0.41V and the flat –

band voltage V_{FB} = 0V. The value of the threshold voltage V_T is

a) -0.82 V b) -0.41 V
c) 0.41 V d) 0.82 V

Q.114 In a semiconductor it is observe that three quarter of the current is carried by electrons and one quarter by holes ,determine the ratio of electrons to holes in the semiconductor .

Q.115 Calculate the diffusion current in a piece of germanium having concentration gradient of 1.5×10^{22} electrons $/m^3$ and $D_n = 0.0012 m^2/s$

Q.116 A sample of germanium is doped with 10^{20} donor atoms$/m^3$ and 5×10^{21} acceptor atoms$/m^3$. Find the total conduction current density if the resistivity of intrinsic germanium at 300 K is 0.6 Ωm with an applied field of 0.02 V/m. Determine the ratio of electrons and holes if the mobility of electrons is two times the mobility of holes at 300K.

Q.117 In a semiconductor at room temperature (300K) the intrinsic carrier concentration and resistivity are $1.5 \times 10^{16}/m^3$ and $2 \times 10^3 \Omega m$ respectively. It is converted to a extrinsic semiconductor with doping concentration of $10^{20}/m^3$. For the extrinsic semiconductor calculate

a) Minority carrier connect ration
b) Resistivity
c) Shift in the Fermi level due to doping
d) Minority carrier concentration when its temperature is increased to a value at which the intrinsic concentration n_i doubles.

Assume

(i) mobility of majority and minority carriers to be the same

(ii) $\frac{KT}{q} = 26\text{mV}$ at room temperature

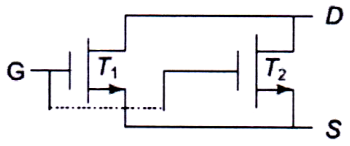
Q.118 The donor concentration in n-type silicon is 1 atom per 10^8 atoms. Find the temperature at which the Fermi level coincides withthe edge of the conduction band assuming that effective mass is equal to the true mass.

Q.119 An n-type semiconductor has its Fermi level 0.25 eV below the conduction band edge. Estimate its dopant, majority, and minority carrier concentrations in equilibrium at room temperature. Assume $n_i = 1.6 \times 10^{16}/\text{m}^3$.

Q.120 Calculate the minimum value of V_{DS} required for an nMOSFET to operate in the pinch-off when $V_{GS} = 1\text{V}$ with $V_T = -2\text{V}$ and $I_{DSS} = 10\text{ mA}$.

Q.121 Two IGFET are connected in parallel to form composite IGFET as shown in Fig Obtain the g_m of the composite IGFET if the drain current of each IGFET is described as

$$I_D = 10 \times 10^{-3}\left(1 + \frac{V_{GS}}{5}\right)^2$$



Q.122 Obtain the minimum value of V_{DS} of an n-channel JFET operating in the pinch –off region with $V_{po} = -4\text{V}, V_{GS} = -2\text{ V}$ and $I_{DSS} = 10\text{mA}$. Calculate the corresponding value I_D

Q.123 For a JFET obtain change in the drain current for $V_{DS} = 3\text{V}$ and corresponding change in the $V_{GS}$from-2V to -1V.

Q.124 Calculate the drain current of an nMOS transistor for $V_{GS} = 0\ V, 1\ V$ and 2 V with the device parameters as $W = 5\mu m, L = 1\mu m, V_{DS} = 0.1V,$ $V_{th} = 1V, \mu_n C_{ox} = 25\mu A/V^2$

Q.125 What would be the output resistance at collector current of 1 mA of a BJT having early voltage of 200V?

Q.126 Calculate the mobility of electron in an N-MOS transistor with the device parameters as
$\frac{W}{L} = 1, V_{GS} = 4VV_{th} = 1.99V,$
$(V_{DS} = 4V\varepsilon_{ox} = 3.97\varepsilon_o, I_D = 144\mu A, t_{ox} = 400A^o)$

Q.127 An enhancement –type transistor with $C_{ox}\mu_n \frac{W}{L} = 0.2\mu A, V_{th} = 2V$ and $\lambda = 0.02/V$ operators $V_{GS} = 4V$ Obtain drain current for ($V_{DS} = 2V$ and 5V and the drain resistance at this value of V_{GS}.

Q.128 Calculate contact potential of a Ge diode having donor impurity concentratio $N_D = 10^{22}/m^3$ acceptor impurity concentration $N_A = 10^{24}/m^3$ and intrinsic concentration $2.5 \times 10^{19}/m^3$

Q.129 If I_B and I_C of any BJT are 1mA and 100 mA respectively, determine its current amplification ratio in CB and CE configurations.

Q.130 If the quiescent collector current of an n-p-n transistor for the base emitter voltage $V_{BE} = 0.7$ is $I_C = 1mA$ what would be the new value of V_{BE} at $I_C = 0.1mA$?

Q.131 What would be the value of leakage current of a transistor at *75°C* ,if the leakage current is $I_{CBO} = 15nA$ at 25°C?

Q.132 Accidentally the emitter and collector leads of an npn transistor have been connected in the inverse mode. The resulting emitter and base currents from this configuration are 5 mA and 1 mA. What would be the value of a_R and β_R ?

ANSWER KEY:

1	2	3	4	5	6	7	8	9	10	11	12	13	14
(d)	(a)	(c)	(b)	(a)	(d)	(b)	(c)	(b)	(c)	(d)	(c)	(b)	(a)
15	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**	**26**	**27**	**28**
(c)	(c)	(d)	(d)	(d)	(c)	(d)	(b)	(c)	(b)	(b)	(c)	(a)	(d)
29	**30**	**31**	**32**	**33**	**34**	**35**	**36**	**37**	**38**	**39**	**40**	**41**	**42**
(d)	(c)	(a)	(a)	(a)	(a)	(b)	(c)	(d)	(c)	(b)	(b)	(c)	(c)
43	**44**	**45**	**46**	**47**	**48**	**49**	**50**	**51**	**52**	**53**	**54**	**55**	**56**
(a)	(C)	(a)	(c)	(b)	(b)	(c)	(a)	(a)	(c)	(a)	(d)	(b)	(c)
57	**58**	**59**	**60**	**61**	**62**	**63**	**64**	**65**	**66**	**67**	**68**	**69**	**70**
(c)	(c)	(a)	(d)	(d)	(a)	(c)	(c)	(b)	(a)	(b)	(c)	(c)	(c)
71	**72**	**73**	**74**	**75**	**76**	**77**	**78**	**79**	**80**	**81**	**82**	**83**	**84**
(b)	(b)	(b)	(a)	(d)	(a)	(d)	(b)	(d)	(d)	(a)	(a)	(b)	(c)
85	**86**	**87**	**88**	**89**	**90**	**91**	**92**	**93**	**94**	**95**	**96**	**97**	**98**
(a)	(d)	(a)	(c)	(c)	(c)	(b)	(c)	(d)	(a)	(b)	(b)	(a)	(b)
99	**100**	**101**	**102**	**103**	**104**	**105**	**106**	**107**	**108**	**109**	**110**	**111**	**112**
(a)	(c)	(c)	(a)	(c)	(c)	(c)	(b)	(a)	(d)	(d)	(c)	(c)	(d)
113	**114**	**115**	**116**	**117**	**118**	**119**	**120**	**121**	**122**	**123**	**124**	**125**	**126**
(d)	*	*	*	*	*	*	*	*	*	*	*	*	*
127	**128**	**129**	**130**	**131**	**132**								
*	*	*	*	*	*								

EXPLANATIONS

Q.1 **(d)**

In intrinsic semiconductor n=p & both take part in conduction.

Q.2 **(a)**

1) For conductors and conduction band and valence band overlaps at room temperature.
2) For insulators the forbidden gap is larger than for semiconductors.

Q.3 **(c)**

With increase in intensity more number of electrons and holes are generated and conductivity increases i.e. resistance decreases.

Q.4 **(b)**

According to mass action law

$$p = \frac{n_i^2}{n}$$

$$= \frac{\left(2.5\times10^{13}\right)^2}{6.25\times10^{18}}$$

$$= 10^8 / cm3$$

Q.5 **(a)**

$$E = 100\,\frac{V}{m}$$

$$V_d = 5\,\frac{m}{s}$$

$$\mu = \frac{V_d}{E} = \frac{5}{100} = 0.05\,\frac{m^2}{V-sec}$$

Q.6 **(d)**

$$R_H = \frac{1}{nq}$$

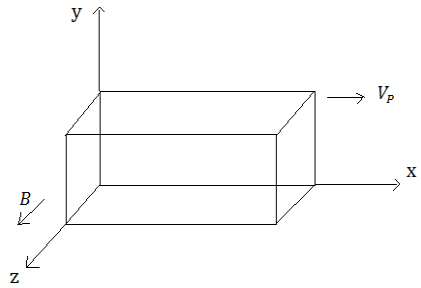
For metals n(electron concentration) is very large as compared to semiconductor.
Therefore, R_H is small

Q.7 **(b)**

$\sigma = nq\mu_n + pq\mu_p$

n(electron concentration) depends on N_c
(density of states in conduction band)

Q.8 **(c)**



Holes will experience a force in downward direction, a positive voltage in negative y direction and negative voltage in positive y direction.

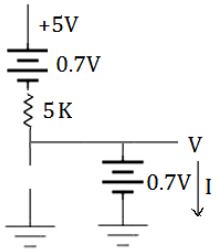
Q.9 **(b)**

$$R(T) = R(0℃)(1+\alpha T)$$

$$1.1 = 1(1+\alpha T)$$

$$\alpha T = 0.1 \Rightarrow T = \frac{0.1}{\alpha} = \frac{0.1}{10^{-3}} = 100℃$$

Q.10 **(c)**



V=0.7 V

$$I = \frac{5-0.7-0.7}{5K} = 720\mu A$$

Q.11 **(d)**

$$V_H = \frac{BIR_H}{w}$$

∴ the hall voltage is not proportional to d.

Q.12 (c)
Gold is used as a recombination agent.

Q.13 (b)

Q.14 (a)

Q.15 (c)
l=1m
$A=0.1\times(10^{-3})^2=10^{-7}m^2$
R=0.171Ω
$R=\frac{\rho l}{A}=\rho=\frac{R\times A}{l}$
$=\frac{0.171\times10^{-7}}{1}=1.71\times10^{-8}\Omega m$

Q.16 (c)
1800 $cm^2/V.s$

Q.17 (d)
$\mu=\frac{V_d}{E}$

Q.18 (d)
$\rho=\frac{1}{\sigma}=\frac{1}{nq\mu_n}$
$=\frac{1}{\frac{1}{1.6}\times10^{22}\times10\times1.6\times10^{-19}}$
$=10000 mho cm^{-1}$

Q.19 (d)
$n_i=\frac{10^{13}}{cm^3}, n=\frac{10^{17}}{cm^3}$
$p=\frac{n_i}{n}=\frac{(10^{13})^2}{10^{17}}=\frac{10^9}{cm^3}$

Q.20 (c)
A photon having $hv \geq E_g$ will only be able to break covalent bonds & generate free charge carriers

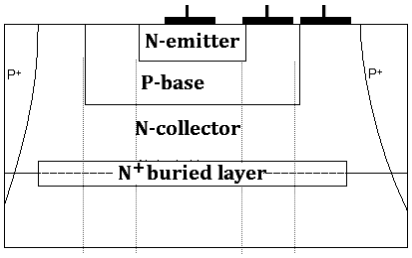
Q.21 (d)
$N_D=\frac{10^{18}}{cm^3}, N_A=\frac{10^{16}}{cm^3}, p=\frac{10^7}{cm^3}$
$p=n_i^2/N_D \quad p=n_i^2/N_A$
$\frac{p}{n}=\frac{N_A}{N_D}\Rightarrow n=\frac{p\times N_D}{N_A}$
$=\frac{10^7\times10^{18}}{10^{16}}=\frac{10^9}{cm^3}$

Q.22 (b)

Q.23 (c)
Complementary error function

Q.24 (b)
Only DG semiconductor is suitable because in direct band gap semiconductors, during recombination energy is released in the form of light.

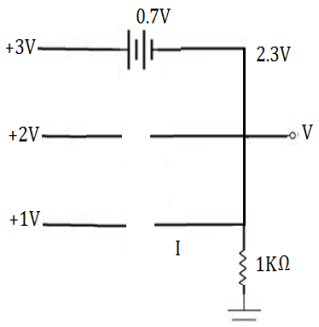
Q.25 (b)



An N^+ buried layer is used in the collector to reduce the collector series resistance.

Q.26 (c)
$E_G=\frac{1.24}{\lambda(\mu m)}$
$=\frac{1.24}{8670\times10^{-4}\mu m}=1.43 ev$

Q.27 (a)



D_2 and D_3 will not conduct.
V=3-0.7=2.3V
And I= $\frac{2.3}{1K} = 2.3mA$

Q.28 (d)

Q.29 (d)
$D = \mu V_T$
$= 0.4 \times 25 \times 10^{-3}$
=0.01

Q.30 (c)
Its cut-in voltage is high

Q.31 (a)
Increase the recombination rate

Q.32 (a)

Q.33 (a)
$\frac{dV_d}{dT} = 2.5mV = 0.0025$

Q.34 (a)

As $C_D = \frac{\tau \times I_0 e^{\frac{V_d}{nV_T}}}{nV_T}$

$\therefore C_D$ increases exponentially with V_d

Q.35 (b)
Highly temperature sensitive because it is minority carrier current & minority carries concentration is sensitive to temperature.

Q.36 (c)
A larger leakage current

Q.37 (d)

$E_G = \frac{hc}{\lambda}$

Q.38 (c)

$C_T = \frac{\in .A}{\sqrt{\frac{2\in}{q}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)(V_0 + V_{RB})}}$

Q.39 (b)
Positive and negative ions on either side

Q.40 (b)

Q.41 (c)
Zener diode has constant voltage across it when used in Reserve bias.
Tunnel diode is used in switching circuit.
Varactor diode is used in tunning circuit.

Q.42 (c)

$C_j = \frac{\in .A}{\sqrt{\frac{2\in}{q}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)(V_0 + V_{RB})}}$

Q.43 (a)

Q.44 (c)

$g = \frac{I_f}{nV_T}$

Q.45 (a)
Both the CB and EB junctions are forward biased.

Q.46 (c)

$I_{CEO} = (1+\beta) I_{CBO}$
$= \left(\frac{1}{1-\alpha}\right) I_{CBO}$

Q.47 (b)

$\alpha = 0.99, \beta = \frac{\alpha}{1-\alpha} = \frac{0.99}{0.01} = 99$

Q.48 (b)

$I_c = \frac{V_{CC} - V_{CE}}{R_C}$

$$= \frac{10-0.3}{1000} = 9.7\text{mA}$$

Q.49 (c)

Q.50 (a)

$$I_{CEO} = \frac{1}{1-\alpha} I_{CO} = \frac{0.5\mu A}{1-0.995}$$

$$I_{CEO} = 100\mu A$$

Q.51 (a)

Double for every 10°C rise in temperature.

Q.52 (c)

$$I_c = I_{co} e^{\frac{V_{BE}}{V_T}}$$

$$5\text{mA} = I_{co} e^{\frac{20\text{mV}}{V_T}}$$

$$30\text{mA} = I_{co} e^{\frac{30\text{mV}}{V_T}}$$

$$\frac{5\text{mA}}{30\text{mA}} = \frac{I_{co} e^{\frac{20\text{mV}}{V_T}}}{I_{co} e^{\frac{30\text{mV}}{V_T}}}$$

$$\frac{1}{6} = e^{\frac{(20-30)}{V_T}}$$

$$\therefore V_T = 5.6\text{mVa}$$

Now, for $V_{EB} = 40\text{mV}$

$$I_c = I_{co} e^{\frac{40\text{mV}}{V_T}}$$

$$\frac{5\text{mA}}{I_c} = \frac{I_{co} e^{\frac{20}{V_T}}}{I_{co} e^{\frac{40}{V_T}}} = 0.028a$$

$$I_c = 177\text{mA} \approx 180\text{mA}$$

Q.53 (a)

Q.54 (d)

$$V_{CE} < \frac{1}{2} V_{CC}$$

Q.55 (b)

I_{DS} = positive maximum at $V_{GS} = 0$

Q.56 (c)

Q.57 (c)

Zero drain current

Q.58 (c)

Polycrystalline silicon is used to reduce V_T

Q.59 (a)

Lower off-set voltage

Q.60 (d)

No cut-off input voltage

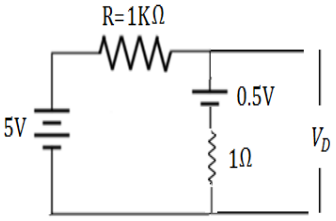
Q.61 (d)

In MOSFET, there is isolation (SiO_2) in between gate and source.

Q.62 (a)

I_D is due to majority charge carries and their mobility decreases with temperature

Q.63 (c)



$$I_0 = \frac{5-0.5}{1\text{K}+1\Omega} = 4.496\text{mA}$$

$$V_d = 0.5 + 4.496\text{mA} \times 1\Omega$$

$$\approx 0.5\text{V}$$

Q.64 (c)

Dynamic drain resistance

Q.65 (b)

Pinch off would occur at

$$V_{DSsat} = V_{GS} - V_T$$

$$= 3 - 0.5 = 2.5\text{V}$$

Q.66 (a)

BJT in CB mode $\Longrightarrow R_i \approx 10\Omega$

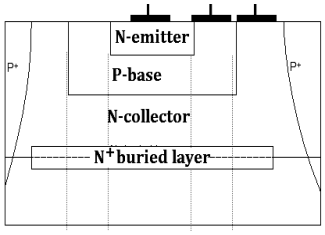
BJT in CE mode $\Longrightarrow R_i =$ few KΩ

JFET$\Longrightarrow R_i = 10^6$ to $10^8\Omega$

MOSFET$\Longrightarrow R_i = 10^{10}$ to 10^{15}

Q.67 (b)
The drain end is more reverse biased than source end

Q.68 (c)



Collector is a part of epitaxial layer & base & emitter are diffused into epi layer.

Q.69 (c)
Isolation

Q.70 (c)

$$E_E = \frac{1}{2}mV^2$$

$$V = \sqrt{\frac{2EF}{m}} = 139\times10^6 \frac{m}{sec}$$

Q.71 (b)

$$L = \sqrt{D\tau}$$

$$D = \mu V_T$$

$$\therefore L = \sqrt{\mu V_T \tau}$$

$$= \sqrt{0.36\times0.0256\times340\times10^{-6}}$$

L=1.77mm

Q.72) (b)
When n-type semiconductor heated at one end, the electrons gain more energy and move to the other end of the material & the heated end becomes positive.

Q.73 (b)
Doping decreases the relaxation time of electrons

Q.74 (a)

Q.75 (d)
Mobility of holes is less than mobility of electrons, due to decrease in electrons concentration conductivity decrease upto certain doping level.

Q.76 (a)

Q.77 (d)

$$V_H = \frac{BIR_H}{w} \text{ so } V_H \propto I$$

Q.78 (b)
1 –f(E)

Q.79 (d)
Let, T_1 =300K be the initial temperature andT_2=310K the initial temperature
At, 300K,

$$kT_1 = \frac{T_1}{11600} = \frac{300}{11600} = 0.0259V$$

$$kT_2 = \frac{T_2}{11600} = \frac{310}{11600} = 0.0267V$$

The factor by which n_i increases is calculate from eq

$$n_i = A_0 T^{\frac{3}{2}} \exp\left(\frac{-E_G}{2kT}\right)$$

$$\frac{n_{i2}}{n_{i1}} = \frac{(T_2)^{\frac{3}{2}} \exp\left(\frac{-E_G}{2k_{T2}}\right)}{(T_1)^{\frac{3}{2}} \exp\left(\frac{-V_G}{2k_{T1}}\right)}$$

$$= \left(\frac{310}{300}\right)^{\frac{3}{2}} \exp\left[\frac{1.11}{2}\left(\frac{-1}{0.0267} + \frac{1}{0.0259}\right)\right]$$

$$= 2.0$$

Q.80 (d)

Q.81 (a)

Q.82 (a)

Q.83 (b)

Q.84 (c)
Positive and negative ions do not move.

Q.85 (a)
Non-availability of free electrons

Q.86 (d)
Remains at the centre of the forbidden gap

Q.87 (a)
Both positive and negative charge carries take part in conduction and total conductivity is addition of conductivity due to both.

Q.88 (c)

Q.89 (c)

Q.90 (c)

$$C_{ox} = \frac{\in_{SiO_2}}{t_{ox}} \approx 6.9 \frac{mF}{m^2}$$

$$= \frac{3.9 \times 8.85 \times 10^{-12}}{5nm}$$

$$C_{Dmin} = \frac{\in_{Si}}{xd_{max}}$$

$$= \frac{12 \times 8.85 \times 10^{-12}}{61nm} = 1.74 \frac{mF}{m^2}$$

$$C_{min} = \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_{Dmin}}} \approx 1.39 \frac{mF}{m^2}$$

Q.91 (b)

Q.92 (c)

Q.93 (d)
Upto saturation time the diode will conduct heavily and the current through diode will be approximately 100 mA but in reserve direction.

Q.94 (a)

Q.95 (b)
The reserve current when large reserve voltage is applied is called reserve saturation current

$$I_0 = 2 \times 10^{-7}$$

$$I_f = I_0 \exp\left(\frac{V_d}{V_T}\right)$$

$$V_T = \frac{KT}{q}$$

$$I_f = I_0 \exp\left(\frac{qV_d}{KT}\right)$$

Q.96 (b)

Q.97 (a)

Q.98 (b)

$$n_i = 2.5 \times 10^{13}, \mu_n = 3800, \mu_n = 1800$$

$$\sigma = n_i q(\mu_n + \mu_n)$$

$$= 0.0224 \text{ S/cm}$$

Q.99 (a)
As b is large, neglect I_B and $I_C \approx I_E$

$$-1.2V + 0.7V + I_C \times 0.45k\Omega = 0$$

$$I_C = \frac{1.2 - 0.7}{0.45k\Omega}$$

$$= 1mA$$

Q.100 (c)

Q.101 (c)
All the resistors are made due to base diffusion because base has high resistivity

Q.102 (a)

Q.103 (c)

Q.104 (c)

$$\alpha = 0.98$$

$$\alpha = \frac{dI_C}{dI_E} \Rightarrow dI_C = \alpha dI_E$$

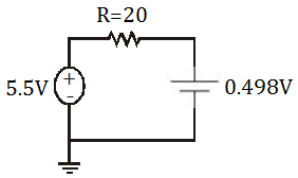
$$= 0.98 \times 5$$

$$= 4.9mA$$

Q.105 (c)

$$E = \frac{V}{W} = \frac{0.1}{10^{-6}}$$

Q.106 (b)



$$I=\frac{5.5-0.498}{20}=250\text{mA}$$

Q.107 (a)

Q.108 (d)

B=2 Tesla, w=0.5mm, I=40A

$$R_H=\frac{1}{qn}=\frac{1}{1.6\times10^{-19}\times10\times10^{28}}$$

$$V_H=\frac{BIR_H}{w}=10\mu V$$

Q.109 (d)

Q.110 (c)

$$\frac{D}{\mu}=V_T=\frac{20}{1600}=12.5\text{mV}$$

Q.111 (c)

In p-well fabrication, a p-well diffused in n-substrate. The p-well is then used as substrate for n-channel MOSFET

Q.112 (d)

$$p=\frac{n_i^2}{N_D}=\frac{\left(10^{16}\right)^2}{10^{26}}=10^6/\text{m3}$$

Q.113 (d)

$V_T = V_{FB} - 2\emptyset_F$

$= 0 - 2 \times -0.41$

=0.82V

Q.114 ()

Total current = $I = I_n + I_p$

As per question $I_n=\frac{3I}{4}$ and $I_p=\frac{I}{4}$

$v_n + 3v_p$

$I_n = n_n q v_n A$ and $I_p = p_n q v_p A$

$$\frac{I_n}{I_p}=\frac{n_n q v_n A}{p_n q v_p A}=\frac{n_n v_n}{p_n v_p}=\frac{n_n\times3v_p}{p_n v_p}$$

$$=\frac{3n_n}{p_n}=\frac{(3/4)I}{(1/4)I}=3$$

$n_n = p_n$

The ratio of electros to holes present in the semiconductor is equal.

Q.115 (2.28)

$$J=qD_n\left(\frac{d_n}{d_x}\right)\text{amp}/\text{m}^2$$

$$=1.6\times10^{-19}\times0.0012\times1.5\times10^{22}$$

$$=2.28\text{A}/\text{m}^2$$

Q.116 (0.05)

$$\sigma_i=n_i q(\mu_n+\mu_p)$$

$$=2.5\times10^{19}\times1.6\times10^{-19}(2\mu_p+\mu_p)$$

$$3\mu_p=\frac{1}{0.60\times2.5\times1.6}=\frac{1}{2.4}$$

$$\mu_p=\frac{1}{7.2}=0.1389\text{m}^2/\text{V}_S$$

$$\mu_n=2\times0.1389\text{m}^2/\text{V}_S$$

$$=0.2778\text{m}^2/\text{V}_S$$

Also

$$p-n=N_A-N_D=5\times10^{19}-10^{20}$$

$$=-(10-5)10^{19}=-5\times10^{19}/\text{m}^3$$

$$np=n_i^2=\left(2.5\times10^{19}\right)^2=6.25\times10^{38}$$

= 0

$$p-\frac{6.25\times10^{38}}{p}=-5\times10^{19}$$

Or,

$$p^2+5\times10^{19}p-6.25\times10^{38}=0\text{A}$$

$$p=1.035\times10^{19}/\text{m}^3$$

$$n=p-\left(N_A-N_D\right)$$

$$=1.035\times10^{19}-\left(-5\times10^{19}\right)$$

$$=6.035\times10^{19}/\text{m}^3$$

$$J = J_n + J_p = \left(n\mu_n + p\mu_p\right)qE$$
$$= \left(6.035\times0.2778 + 1.035\times0.1389\right)10^{19}$$
$$\times1.6\times10^{19}\times0.02$$
$$= \left(1.677 + 0.144\right)0.032$$
$$= 0.0582 A/m^2$$

Q.117 ()

(a) minority × majority carrier concentrations $= n_i^2$

Hence, minority carrier concentration

$$= \frac{\left(1.5\times10^{16}\right)^2}{10^{20}}$$
$$= 2.25\times10^{12} atom/m^3$$
$$\sigma_i = n_i q\left(\mu_n + \mu_p\right)$$
$$= 1.5\times10^{16}\times1.6\times10^{-19}\left(2\mu_n\right)$$
$$= 2.4\times10^{-3}\times2\mu_n$$
$$\mu_n = \frac{\sigma_i}{2.4\times2\times10^{-3}}$$
$$= \frac{1}{4.8\times10^{-3}\times2\times10^{+3}} = 0.104 m^2/V_S$$

(b) Conductivity of extrinsic semiconductor $= \sigma_n = nq\mu_n$

Since doping concentration >>minority concentration only doping concentration will be used. Hence

$$\sigma_n = 10^{20}\times1.6\times10^{-19}\times0.1042$$
$$= 1.67 mho/m$$
$$\text{resistivity} = \frac{1}{\sigma_n} = 0.6\Omega m$$

(c) $E_F - E_i = KT\,In\left(\frac{n_o}{n_i}\right)$

$$= 26\times10^{-3}\times In\left(\frac{10^{20}}{1.5\times10^{16}}\right)$$
$$0.026 In\left(6.67\times10^2\right) = 0.23eV$$

(d) Minority carrier concentration

$$= \frac{\left(2\times1.5\times10^{16}\right)^2}{10^{20}}$$
$$= 9\times10^{12} atoms/m^3$$

Q.118 (0.226)

$$N_D = \frac{5\times10^{28}}{1\times10^8} = 5\times10^{20} atom/m^3$$

The Fermi level

$E_F = E_C for N_D = N_C$

It is known that

$$N_C = 4.82\times10^{21}T^{3/2}/m^3$$
$$5\times10^{20} = 4.82\times10^{21}T^{3/2}/m^3$$
$$T^{3/2} = \frac{5\times10^{20}}{4.82\times10^{21}} = 0.1037$$
$$T \cong \left(0.1073\right)^{2/3} = \left(0.1073\right)^{0.666}$$
$$= 0.226K$$

Q.119 ()

$$n_n = N_{C^{\times e}}^{-\left(\frac{E_C - E_F}{KT}\right)}$$
$$N_C = 2\left(\frac{2\pi mKT}{h^2}\right)^{3/2}$$
$$E_C - E_F = 0.25eV,$$
$$N_C(300K) = 2.9\times10^{25}/m^3$$
$$n_n = 2.9\times10^{25}e^{-\frac{0.25}{8.62\times10^{-5}\times300}}$$
$$= 2.9\times10^{25}e^{-\frac{0.25}{8.62\times10^{-5}\times300}}$$
$$= 2.9\times10^{25}e^{-9.66744} = \frac{2.9\times10^{25}}{e^{-9.66744}}$$
$$= \frac{2.9\times10^{25}}{1.5795\times10^{14}} = 1.83\times10^{21}/m^3$$
$$p_n = \frac{n_i^2}{n_n} = \frac{2.56\times10^{32}}{1.83\times10^{21}} = 1.39\times10^{11}/m^3$$

Q.120 (3)

It is known that foran N-MOSFET the V_p is a negative number. Hence, the minimum values of V_{DS} required to keep it in saturation is

$V_{DS} \geq V_{GS} - V_p = 1 - (-2) = 3V$

Q.121 ()

Since both IGFETs are connected in parallel, the resulting drain current of the composite IGFET is

$$I'_D = 2\times10\times10^{-3}\left(1+\frac{V_{GS}}{5}\right)^2$$

Hence,

$$g_m = \frac{\delta I'_D}{\delta V_{GS}}$$

$$= 2\times2\times10\times10^{-3}\left(1+\frac{V_{GS}}{5}\right)\times\frac{1}{5}$$

$$= 8\times10^{-3}\left(1+\frac{V_{GS}}{5}\right)$$

Q.122 (2.5)

$$V_{DS} \geq V_{GS} - V_{po} = -2-(-4) = 2V$$

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_p}\right)^2$$

$$= 10\times10^{-3}\left(1-\frac{-1}{-2}\right)^2$$

$$= 10\times10^{-3}(1-0.5)^2 = 2.5mA$$

Q.123 (2.02)

For

$V_{GS} = -1V, V_p = V_{GS} - V_{DS}$

$= -1V - 3V = -4V$

Similarly,

For $V_{GS} = -2V, V_p = -3V = -5V$

$$I_{DI} = I_{DSS}\left(1-\frac{V_{GS}}{V_p}\right)^2$$

$$= 10\times10^{-3}\left(1-\frac{-2}{-5}\right)^2$$

$$= 10^{-2}(1-0.4)^2 = 3.6mA.$$

$$I_{D2} = I_{DSS}\left(1-\frac{V_{GS}}{V_p}\right)^2$$

$$= 10\times10^{-3}\left(1-\frac{-1}{-4}\right)^2$$

$$= 10^{-2}(1-0.25)^2 = 5.625mA.$$

$$I_{D2} - I_{DI} = 5.625mA - 3.6mA$$

$$= 2.025mA$$

Q.124 ()

For $V_{GS} = 0V < V_{th} = 1V$

channel does not form ,$I_D = 0$

For $V_{GS} = 2\ V > V_{th} = 1\ V$,

channel forms and the equation of I_D is

As $V_{DS} < (V_{GS} - V_{th})$, therefore it is operating in linear region.

$$I_D = \mu_n C_{ox}\frac{W}{L}\left[(V_{GS}-V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$$= 25\times10^{-6}\frac{5}{1}\left[(2-1)0.1 - \frac{0.1^2}{2}\right]$$

$$= 125\times10^{-6}(0.1-0.005)$$

$$= 125\times11.875\mu A$$

Q.125 (200)

$$r_o = \frac{V_\lambda}{I_C} = \frac{200}{1mA} = 200K\Omega$$

Q.126 (405)

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.97\times8.854\times10^{-14}}{400\times10^{-8}}$$

$$= 0.088\times10^{-6}$$

As $V_{DS} > V_{GS} - V_{th}$ it is operating in saturation

$$I_D = \mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{th})^2$$

$$= 0.088\times10^{-6}\mu_n\times(4-1.99)^2$$

$$\mu_n = \frac{144}{0.355} = 405cm^2/s$$

Q.127 (125)

$V_{GS} - V_{th} = 4 - 2 = 2V$

$= V_{DS} \Rightarrow$ Saturation

$$I_D = \frac{1}{2} C_{ox} \mu_n \frac{W}{L} (V_{GS} - V_{th})^2 (1 + \lambda V_{DS})$$

$$= \frac{0.2}{2} (2)^2 (1 + 0.02 \times 2)$$

$= 0.4(1.04)$

$= 0.416mA$

$$I_{DS} = \frac{1}{2} C_{ox} \mu_n \frac{W}{L} (V_{GS} - V_{th})^2 (1 + \lambda V_{DS})$$

$$= \frac{0.2}{2} (2)^2 (1 + 0.02 \times 5)$$

$= 0.4(1.1)$

$= 0.44mA$

Increase in $I_D = \Delta I_D$

$= 0.44 - 0.416 = 0.024mA,$

$\Delta V_{DS} = 5 - 2 = 3V$

$$\dot{r}_d = \frac{3V}{0.024mA} = 125K\Omega$$

Q.128 (0.43)

$$V_0 = V_T In \frac{N_D N_A}{n_i^2}$$

$$= 0.026 In \frac{10^{22} \times 10^{24}}{6.25 \times 10^{38}}$$

$$= 0.026 In \frac{10^8}{6.25}$$

$$= 0.026 \left(In 10^8 - In 6.25 \right)$$

$= 0.026(8 \times In10 - In6.25)$

$= 0.026(8 \times 2.3 - 1.83)$

$= 0.026 \times 16.57 = 0.431$ V

Q.129 (0.99)

$$I_c = \beta I_B + (1 + \beta) I_{CO} \cong (1 + \beta) I_B$$

$= \beta \times 1mA = 100mA$

$\therefore \quad \beta = 100$

The current amplification ratio in CE $= \beta = 100$

The current amplification ratio in CB $= \propto$ and it is expressed as

$$\alpha = \frac{\beta}{1 + \beta} = \frac{100}{101}$$

$= 0.990099 = 0.99$

Q.130 (0.64)

$I_C = I_S \exp^{V_{BE}/V_T}, 1 = I_S \exp^{0.7/0.026}$

$= I_S \exp^{26.923} = 4.93 \times 10^{11} I_S$

$\therefore I_S = 2 \times 10^{15} A$

$I_C = I_S \exp^{V_B/0.026}$

$= 2 \times 10^{15} \exp^{V_B/0.026}$

$\Rightarrow 0.1 \times 10^{-3}$

$= 2 \times 10^{15} \exp^{V_B/0.026}$

$\Rightarrow V_{BE} = 0.026 \times 24.6353 = 0.64V$

Q.131 ()

$I_{CBO1} = I_{CO} \exp^{K_2 t_1},$

$I_{CBO2} = I_{CO} \exp^{K_2 t_2},$

$$\frac{I_{CBO2}}{I_{CBO1}} = \exp^{K_2 (t_2 - t_1)},$$

$I_{CBO2} = I_{CBO1} \exp^{K_2 (t_2 - t_1)}$

$I_{CBO2} = 15nA \exp^{0.07 \times 50}$

$= 15nA \exp^{3.5} = 15 \times 10^{-9} \times 33.12$

$= 0.5 \times 10^{-6} A$

Q.132 (0.833)

$$\beta_R = \frac{I_C}{I_B} = 5, \alpha_R = \frac{I_C}{I_E} = \frac{5}{5+1} = 0.833$$